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AN ANALOG-TO-DIGITAL CONVERTER FOR REAL-TIME COMPUTATION UTILIZING THE ERA 1101 DIGITAL COMPUTER

A THESIS

Presented to

the Faculty of the Graduate Division

by

Richard Laman Nickelson

In Partial Fulfillment

of the Requirements for the Degree

Master of Science in Electrical Engineering

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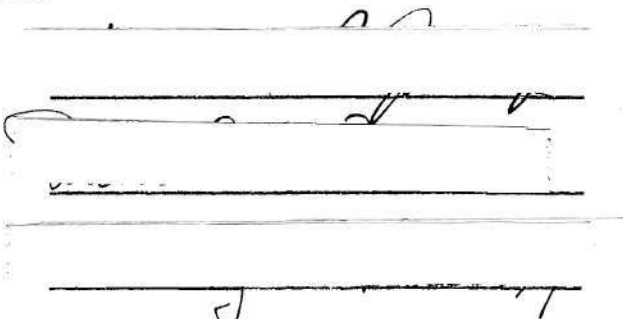

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To the staff of the Rich Electronic Computer Center and to the members of my reading committee, Dr. D. C. Fielder and S. P. Lenoir, I express my appreciation for their interest and enlightening criticism.

And to my fiancée, Joyce Rice, I express my appreciation for her patience, understanding, and assistance during the preparation of the final draft.

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SUMMARY

This study examines the problems associated with real-time digital computation, with special emphasis placed upon the choice of a system which is compatible with the speed of operation and electrical design of the ERA 1101 digital computer, and which has computational accuracy comparable to the accuracy of the continuous input signal. Economy of operation and construction are also considerations in the final choice of a system.

Recently, considerable attention has been directed toward the utilization of the speed and accuracy of modern digital computers for real-time computation. In order to use a digital computer (which can assimilate data only if it has discrete levels) as part of a physical system (which generally has continuous parameters), it is necessary to be able to express a continuously varying (analog) input in terms of the machine "language". The digital computer may then perform mathematical operations upon the resulting quantized input data, and the digital results of computation may be converted to analog form for immediate use in the physical system. However, problems of speed and accuracy plague such analog-to-digital and digital-to-analog converters.

A survey of the literature revealed several possibilities for converter design. A class of converters which uses the servomechanism approach in design procedure was chosen as the most promising. From

this class, a cascaded-stage comparison coder and a successive-approximation comparison coder are examined in detail.

Both of these converters theoretically meet the speed and accuracy requirements established in the initial statement of the problem. Because of practical considerations, however, the successive-approximation comparison coder is chosen for the converter circuits to be used with the ERA 1101 computer. Circuit diagrams of the complete coder are presented and the functioning of the various sections is explained in some detail. The results of the laboratory evaluation of a transistorized differential amplifier for conversion accuracy are also presented. In addition, a block diagram showing the necessary additions to and modifications of the ERA 1101 computer is developed.

Real-time digital computers are proving to be valuable tools for simulation engineers in the study of sampled-data systems. For this reason, and because of the many other possibilities for real-time digital computation, it is felt that the described converters and control circuits would prove to be valuable additions to the ERA 1101 digital computer.

CHAPTER I

INTRODUCTION

Representation of quantities.-- Many engineering problems involve the acquisition of large amounts of data and the subsequent reduction of that data to a useful form. Since physical processes are, in general, continuous, data may be obtained by any of several methods. Take as an example the recording of atmospheric pressure as a function of time. A barometer may be attached to a potentiometer in such a fashion that the wiper of the potentiometer moves as the atmospheric pressure changes. If a constant voltage is then applied across the potentiometer, the voltage appearing at the wiper will be indicative of the atmospheric pressure at any given instant. Assuming that the potentiometer has infinite resolution, the wiper voltage may be recorded on a chart moving at a constant speed as the continuous representation of atmospheric pressure. Such a recording would be called the analog representation of atmospheric pressure.

Another possibility for obtaining information regarding the variation of atmospheric pressure would be to have a technician watch a barometer and keep a written record of pressure readings taken at specified times. This record would be a sampled representation of atmospheric pressure.

If it is desired to know the change in atmospheric pressure between time "A" and time "B", either recording is equally useful,

provided, of course, the technician has made readings at these times. Reference to the continuous chart may show that the barometer reading at time "A" was 29.757 inches of mercury. The technician may have recorded 29.7572 inches of mercury as the reading at time "A". Both of these figures are digital representations of the true barometric pressure at time "A", which is assumed to have been 29.757243 inches of mercury.

Either the analog or the sampled record may assume any of an infinite number of values at any given time. However, there is a practical limit to the number of significant digits which the observer may read from either record.

Modern high-speed electronic digital computers are noted for accuracy in computation, hence it is often desirable to be able to express analog inputs in the "language" of the machine. Many different types of analog-to-digital converters have been designed and constructed for this purpose, but the difficult problems of conversion time and accuracy continue to plague all but the most expensive and complicated systems (1).

Since the nature of the digital computer limits the number of levels which can be expressed to a finite number of digits, the conversion of an analog signal to digital form can only be an approximation. Also, since the digital computer requires a finite amount of time to operate upon any data it receives, data must be supplied in distinct groups at appropriate times. Hence, the input to a digital computer must be in quantized samples.

With reference to the previous example, note that a digital computer would accept the analog input record within the limit of significant digits of the machine and truncate the remainder, much as the technician dropped those digits which were beyond the capacity of his eye to read. Likewise, the machine would accept data only as rapidly as it could assimilate and dispose of previous data. Thus, if the machine required fifty milliseconds to operate upon the digital representation of the barometric pressure at time "A", it would not be able to compute the difference in barometric pressure between time "A" and time "B" if time "B" were thirty-five milliseconds later than time "A".

Uses for analog-to-digital converters.-- Analog-to-digital converters have found acceptance for several uses (1). The previously mentioned example of recording barometric pressures would be an example of a converter-computer combination utilized for data reduction. Other categories include: (1) control systems following programmed instructions, (2) closed-loop control systems, and (3) analog computer simulation in which the digital computer is utilized as an active element.

Object of the study.-- It is the purpose of this study to set forth the design principles for an analog-to-digital converter for use with the ERA 1101 digital computer at the Rich Electronic Computer Center on the campus of the Georgia Institute of Technology (2). This converter would permit the ERA 1101 computer to be used for computation in real time utilizing an analog input. A digital-to-analog converter would also be designed in order to provide a useful analog output.

Computation in real time involves the acceptance of a continuously varying input by the input converter; the acceptance of quantized samples of that input by the computer; the operation upon these samples by the computer; the acceptance of digital results by the output converter; and the conversion of the digital results to analog form by the output converter.

An example of a closed-loop digital control system is the Semi-Automatic Ground Environment (SAGE) system which has gained extensive public attention as a major link in our civil defense system (1). The SAGE system takes advantage of the speed and accuracy of a large-scale digital computer to process radar information detailing the location of unfriendly aircraft to provide interceptor flight-path instructions. The SAGE system may be considered a closed-loop system because the computer is utilized to direct the flight path of the defense interceptors. A block diagram of a typical closed-loop control system utilizing a digital computer is shown in Figure 1.

The digital computer may be used as a versatile function generator in analog computer simulation problems. Unusual functions may be stored in the memory of the digital computer and the digital computer may then be utilized as the active function generator in an analog computer problem. Figure 2 is the block diagram of such a system.

Multiplication, division, and integration are operations which often produce large errors in analog computer problems. The accuracy of the digital computer in performing these operations may be utilized

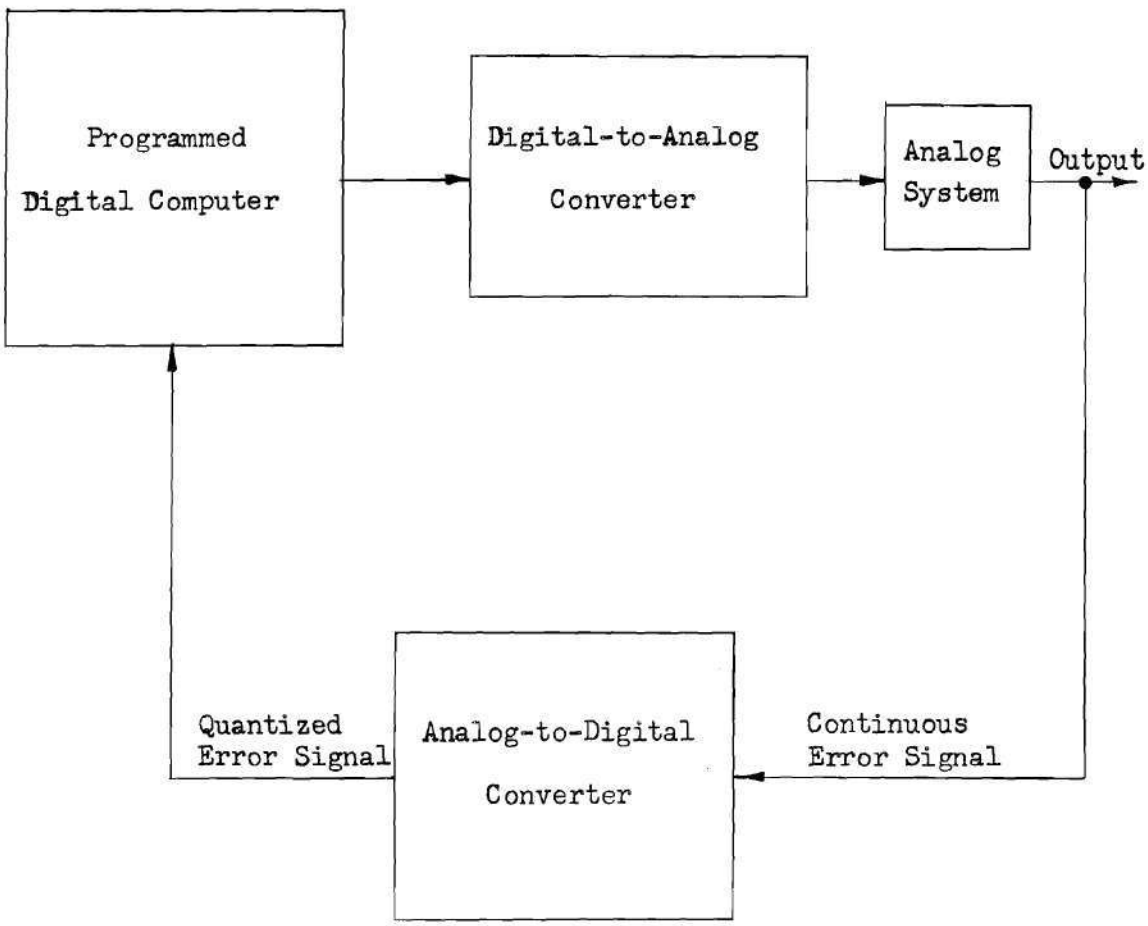
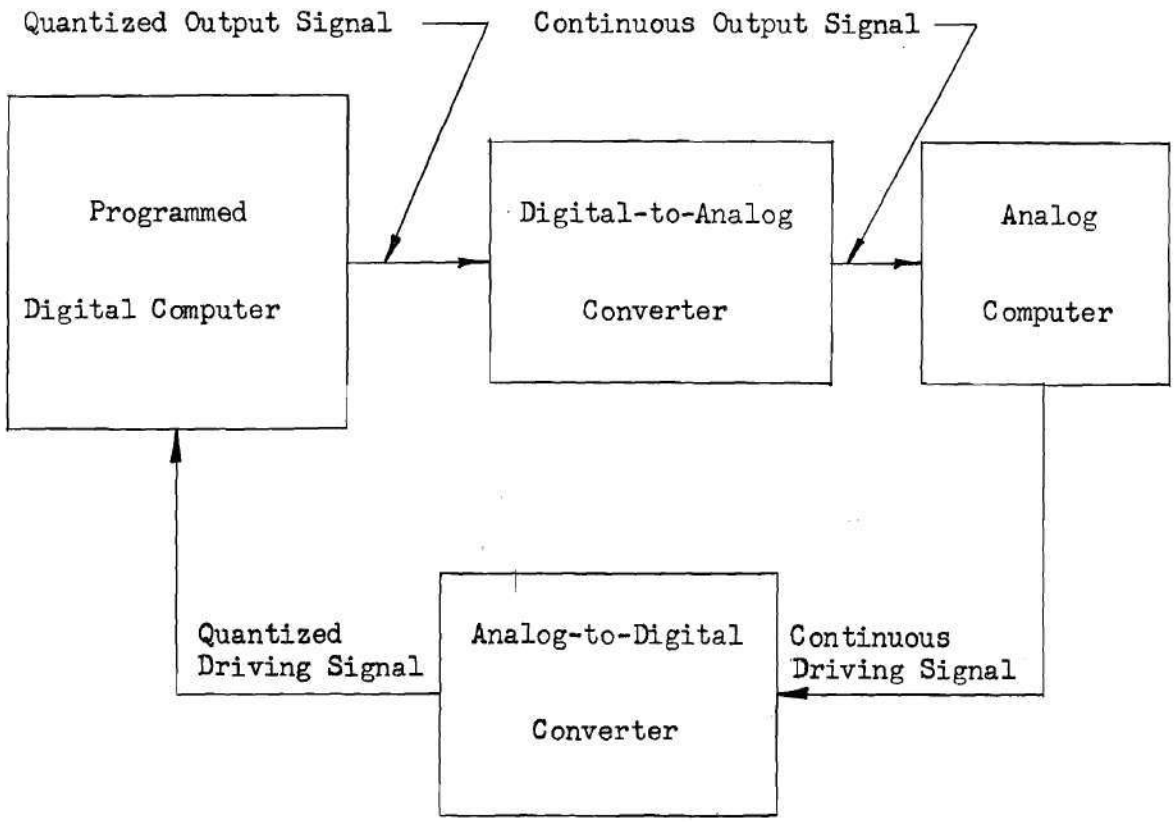
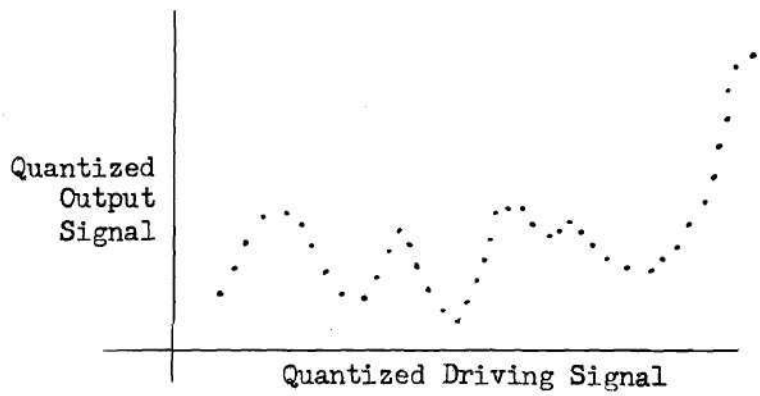


Figure 1. Closed-Loop Control System With
A Digital Computer in the Loop



a. Block Diagram



b. Typical Programmed Function

Figure 2. Digital Computer Utilized as a Function Generator in an Analog Computer Problem

if analog-to-digital and digital-to-analog converters are included as active elements in the system, as shown in Figure 3.

By taking advantage of a multiplexed input-output scheme, more than one control system may be controlled by a single digital computer at the same time. Likewise, a single digital computer may be used for multiplication, division, and integration in an analog computer problem by taking advantage of the same scheme. Many other possibilities exist for the utilization of a digital computer for computation in real time.

Problems involved in digital computation in real time.-- Conversion time and accuracy are problems which plague all but the most expensive and elaborate analog-to-digital converters. Of primary consideration in examining these problems as applied to the design of converters for use with the ERA 1101 computer is the necessity for compatibility.

The input converter must be able to provide inputs as the computer requires them. Hence, the speed of conversion must be compatible with the frequency content of the analog input and the computing speed of the ERA 1101 computer. Likewise, the output converter must be able to operate at a speed which is compatible with the computation speed of the computer.

The converters must not introduce excessive errors in the digital representation of the analog signal and vice versa. Errors due to truncation are necessary evils, but care must be taken to assure that a sufficient number of digits are utilized to represent

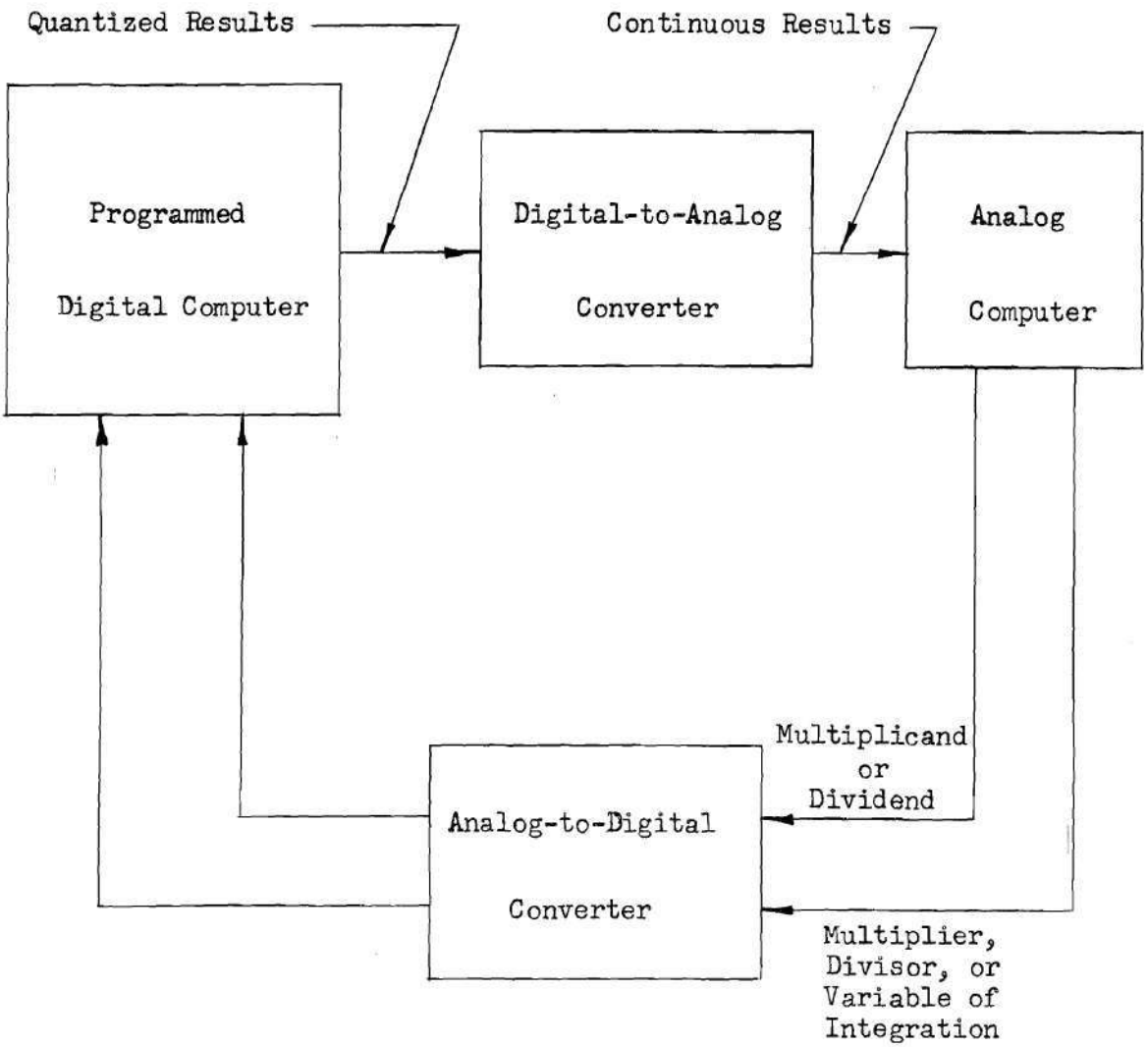


Figure 3. Digital Computer Utilized as a Multiplier, Divider, or Integrator in an Analog Computer Problem

the true analog signal with minimum truncation error. Also, the converters should introduce a minimum of internally generated error. Analog representations of physical variables are usually assumed to be "sufficiently accurate" if they provide resolution which produces no more than 0.1 per cent of full-value error. Hence, this will be assumed to be the maximum allowable error for the converters.

Both conversion time and accuracy are of major importance in determining system stability if the converter-computer combination is to be used in a closed-loop system. An example of the problems which may arise is given by the SAGE system (1):

> All data from the radar sites are in the form of quantized samples, which are transmitted to the computer over telephone lines. Search radar is used and provides scanning on a time basis so each target is seen at a discrete time determined by the position of the rotating antenna and the range delay in receiving the echo. Quantization level and sampling rate of the input data are determined largely by the information capacities of the radars involved. However, the computer also places demands on quantization level and sampling rate because it must use the data in flight path extrapolation. Data taken at insufficient intervals or of low resolution would make it impossible for the computer to provide accurate results and the resulting system would be unstable. Thus, steering information might cause the aircraft to fly an oscillatory path or miss the interception altogether. Conversely, because of the large number of problems being handled simultaneously, too much input data may also cause trouble by overloading the computer. There is therefore a balance between the input quantization levels and sampling rates necessary for system accuracy and stability, and those that might overload the entire system.

Another consideration in the design of the converters is the correspondence between input sampling rates and quantization levels and those of the output. These need not necessarily be on a one-to-one basis, and the system may require a number of input samples to

provide one output. Conversely, the computer may be required to interpolate additional outputs in order to achieve a smooth output.

These problems are treated in detail in the discussion of converter design, following an explanation of the operation and construction of the ERA 1101 digital computer.

CHAPTER II

THEORY OF OPERATION OF THE COMPUTER

System description.-- In order to intelligently design input and output converters to make the ERA 1101 digital computer adaptable to real time computation involving continuously varying input and output signals, it is necessary to gain a working knowledge of the theory of operation of some sections of that computer. A digital computer may be considered to be composed of the following five sections:

1. Input section
2. Storage section (memory)
3. Control section
4. Arithmetic section
5. Output section

These sections generally perform the functions implied by their titles. The input section provides a means for placing a problem in the computer. The storage section retains for later use binary information placed in it. The sequence of manipulations and operations is governed by the control section, while the arithmetic section performs the binary manipulations required to solve a problem. The output section provides the outlet for the result of a computation.

Basically, the philosophy of the computer's operation is that sequentially generated pulses are switched to various stages where

certain events are made to occur. The switching device consists of a gate turned on or off by flip-flops. Most of the circuits of the computer are composed of various combinations of these two fundamental building-blocks. A block diagram of the major components of the computer is shown in Figure 4.

The information to be stored is coded in terms of the binary digits 0 (zero) and 1 (one). Each memory position or "word" is capable of storing 23 bits of numerical information and a sign bit, i.e., each memory word consists of 24 bits of information. At present, the ERA 1101 computer has two storage sections (3). The drum memory has a storage capability of 16,384 words with a maximum access time of approximately 17 milliseconds. The newer magnetic-core memory has a storage capability of 4096 words with a uniform access time of ten microseconds. "Access time" as used here means the amount of time required by the machine to locate any particular memory position and extract the information contained in that position. Either of these memories or both may be used in a single program. Because of the faster access time, the magnetic-core memory will be considered for use in real-time computation.

Selection of a desired memory position for insertion or interrogation of data is accomplished by employing an address consisting of 14 bits. These addresses are given the octal designations 00000, 00001, . . . , 07776, 07777, 10000, 10001, . . . , 37776, and 37777 in the case of the drum memory. The addresses 40000 through 47777 are reserved for the magnetic-core memory.

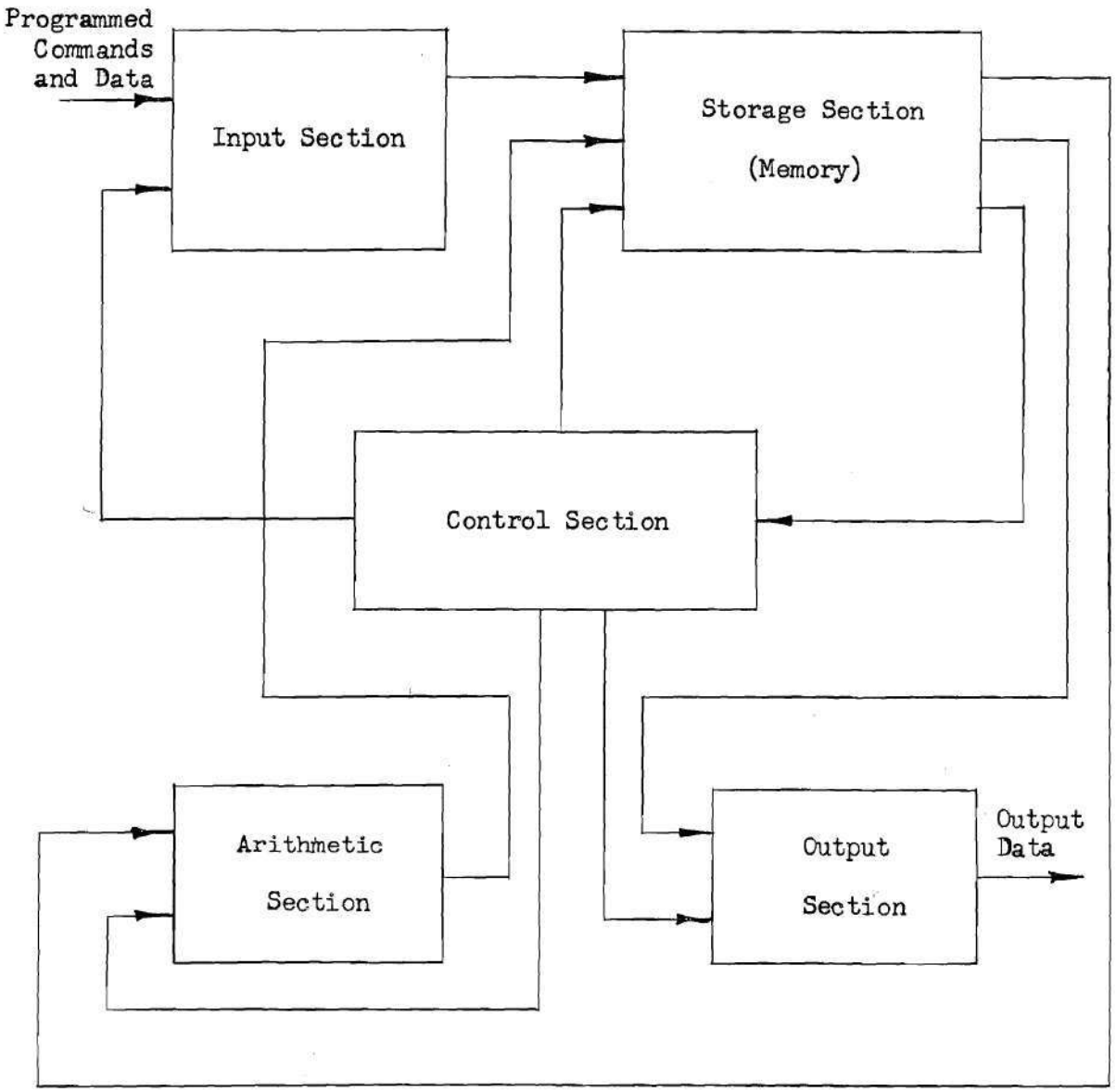


Figure 4. Block Diagram of the ERA 1101 Computer

Insertion of new data at a particular location automatically destroys any information previously contained at that location. A location may be interrogated any number of times without destroying the information contained therein, however.

Computer registers.-- Parallel transmission of binary information is used throughout the computer. All information being operated upon in the computer (excluding data stored in the memory) is contained in flip-flop registers. Data transmission between registers is accomplished by means of gating circuits. The characteristics of a gate are such that a pulse applied at one of two input terminals produces an output pulse only if an enable signal is present on the second input terminal.

The following computer registers are of interest for the problem at hand:

1. Storage Insertion Register (SIR)
2. Program Control Registers (PCR)
   a. Execution Address Register (EAR)
   b. Command Translator Switch (CTS)
3. Program Address Counter (PAK)
4. Storage Address Register (SAR)
5. Accumulator (A)
6. Quotient Register (Q-Register)
7. X-Register

During a computation the PAK keeps track of the memory location containing the next instruction. Normally, instructions are stored in

sequential locations, so the primary function of the PAK is to advance in count each time an instruction is executed. It is possible to deviate from sequential order, however, by means of certain "jump" instructions, in which cases the jump instruction alters the contents of the PAK. After the current instruction has been executed, the contents of the PAK are transmitted to the Storage Address Register (SAR), and a memory read cycle is initiated. Then the next instruction is read from memory to the Program Control Registers (PCR) and the contents of the PAK are increased by one.

Instructions for the computer are designated in octal form (i.e., three bits per octal digit) as shown in Figure 5.

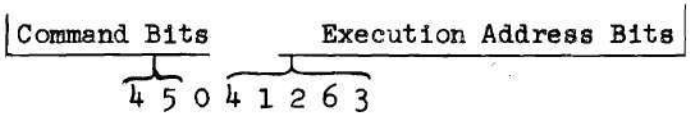


Figure 5. A Typical Machine Instruction

The first six bits of an instruction are called the command bits. A list showing the available commands and explaining the command code is given in the computer instruction manual (2). The final 15 bits contain the memory address at which the command is to be executed. In Figure 5, for example, "45" tells the machine to "JUMP to memory location 41263 to execute the next instruction." After being read out, the instruction is broken into two parts. The first six bits go to the Command Translator Switch (CTS), which then carries out the mathematical or logical operation commanded, while the final 15 bits are sent to the Execution Address Register (EAR). Note that the EAR serves as a storage location for the bits of the

execution address as they are read from storage.

The binary point is located at the right in all registers. This means that the machine treats all numbers as integers. Hence, scale factors must be used to handle non-integral numbers. As mentioned previously, the machine handles both positive and negative numbers, with the left-most bit in a register indicating the sign of a number. The "one's complement" system of representation is used. Thus, negative numbers are expressed as complements of $2^n - 1$, where n indicates the total number of bits in the register. For this reason, the sign bit for a positive number is zero, and for a negative number it is one.

The X-Register and Q-Register have a 24-bit capacity, while the Accumulator has a 48-bit capacity. These registers are the principal components of the arithmetic section.

The Accumulator is the primary operational register of the ERA 1101 computer. It is basically subtractive with end-around borrow. Thus, every number transmitted to the Accumulator will automatically be subtracted from the number there and the resulting difference will remain in the Accumulator after the subtraction. In order to add a number to the Accumulator, it is necessary to transmit its complement to that register. The accumulator also has borrow and circular shift capabilities.

The X-Register has neither additive nor shift properties. It is used to hold numerical data read from storage for use in arithmetic operations.

The Q-Register participates in several arithmetic and logical operations. The quotient is formed there during division and the multiplier is placed in it for multiplication. The Q-Register has circular shift capabilities.

Data to be stored is received by the Storage Insertion Register (SIR) from either the Accumulator or the Q-Register, depending upon the storage instruction. The state of each stage of the SIR will enable the appropriate storage gates, and the sequence initiated by the storage instruction will cause the data to be stored in the specified memory location.

CHAPTER III

THEORY OF ANALOG-TO-DIGITAL CONVERSION

Sampling.-- It has been mentioned previously that sampling the input is frequently necessary for successful analog-to-digital conversion and is utilized in the converters to be described. Obviously, sampling is an operation which can introduce serious error into computations if not applied carefully. This is particularly true in the case of closed-loop systems, where improper sampling may cause serious instability or damage to the system. D. T. Ross has developed an excellent intuitive approach to the problem of sampling, and his work is heavily relied upon in the discussion that follows (1).

Fourier analysis may be applied to any function which satisfies the Dirichlet conditions, i.e., it is at least piecewise continuous, has no infinite discontinuities, and has a finite number of maxima and minima in a period (4). The Fourier analysis of functions shows that such functions may be considered to be composed of a linear combination of simple sinusoids of various amplitudes, phases, and frequencies. For the general non-periodic f(t), the Fourier integral is given by

$$f(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} F(\omega)\, \epsilon^{j\omega t}\, d\omega$$

where

$$F(\omega) = \int_{-\infty}^{\infty} f(t)\epsilon^{-j\omega t}\, dt .$$

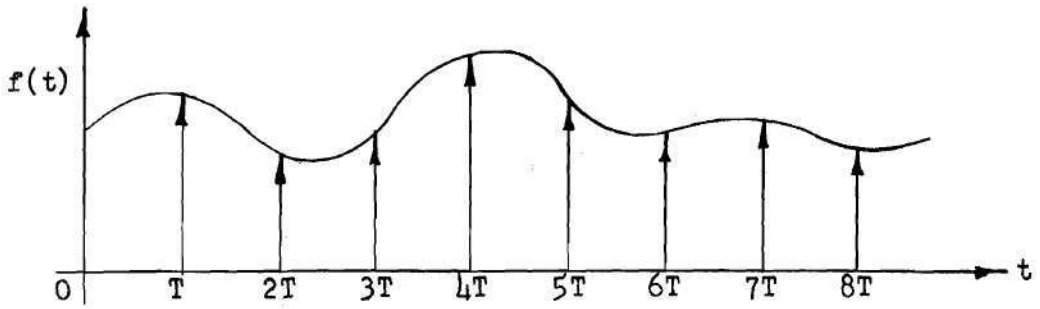
$F(\omega)$ is called the Fourier transform of $f(t)$. The following statement, which is known as Black's Sampling Theorem (5), results from an application of Fourier analysis:

> If $F(\omega) = 0$ for $|\omega| \geq \frac{\pi}{T}$, then $f(t)$ may be completely recovered from $f^*(t)$, where $f^*(t)$ is $f(t)$ sampled at the rate $\frac{1}{T}$.

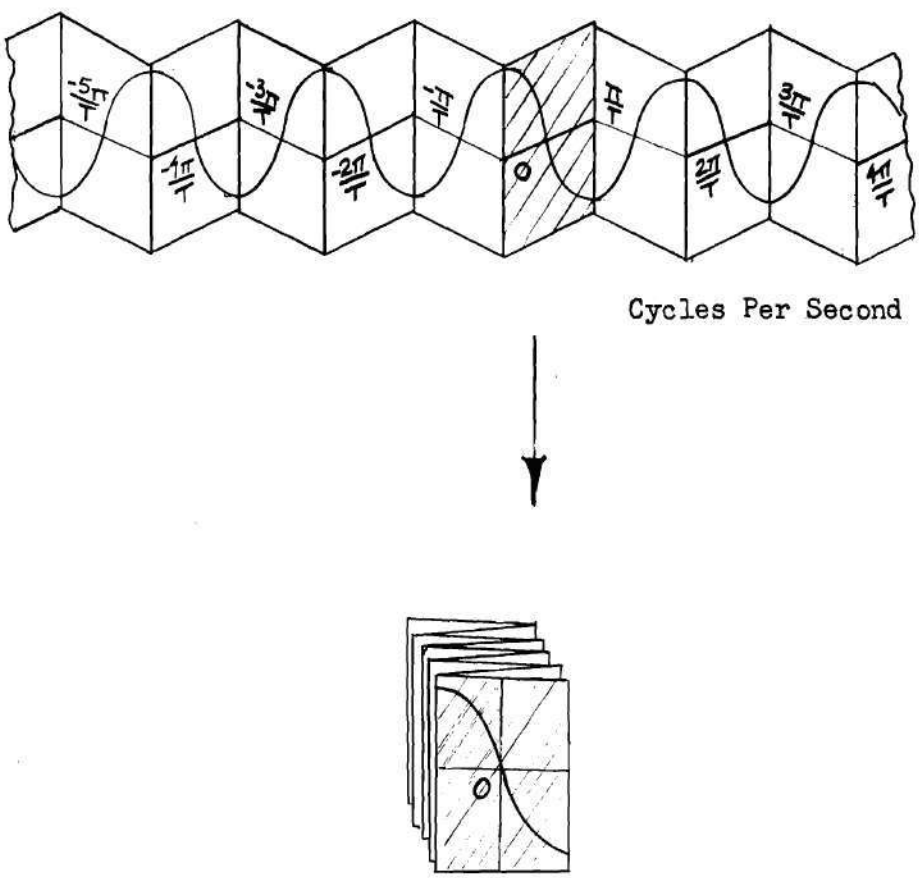
Now, according to the Sampling Theorem, if $f(t)$ is sampled at the rate $\frac{1}{T}$ times per second (see Figure 6), the frequency components of the signal greater than $\frac{\pi}{T}$ radians per second cannot be distinguished from frequencies in the range zero to $\frac{\pi}{T}$ radians per second. Thus, sampling has the effect of placing an "accordion fold" in the frequency scale at every multiple of $\frac{\pi}{T}$. Note, however, that nothing is lost by sampling $f(t)$ under the conditions of the Sampling Theorem since $F(\omega) = 0$ for $\omega \geq \frac{\pi}{T}$ and since $\frac{\pi}{T}$ is the first "fold" resulting from sampling. Because $f(t)$ is uniquely determined by $F(\omega)$, the Sampling Theorem holds.

It is important to note that when $f(t)$ is a function with frequency components greater than $\frac{\pi}{T}$, it is not necessarily possible even to recognize $f(t)$ from $f^*(t)$, much less reconstruct $f(t)$.

Since the frequency components of a signal sampled at the rate of $\frac{1}{T}$ samples per second cannot be distinguished for frequencies greater than $\frac{\pi}{T}$ cycles per second, the sampling theorem may be rephrased as follows: "At least $2f_m$ uniformly spaced samples are needed every second in order to reproduce the signal without distortion." (6)



a. Signal Sampled at T-Second Intervals



b. Folding of Frequency Spectrum Caused by Sampling (1)

Figure 6. Results of Sampling a Signal at a Rate of 1/T Samples Per Second

Here f_m is the highest frequency of interest. Note that the presence of frequencies higher than f_m will cause distortion in the sampled signal. Hence, it is necessary to use a low-pass filter with a cut-off frequency of f_m if the signal contains frequency components higher than f_m.

Laplace transform theory and Z-transform theory prove particularly valuable in the analysis of sampled-data systems. Since these methods are generally known and are treated rather extensively in the literature (7), it will only be mentioned that resort to them may be necessary to determine if a particular control system will be adaptable to use as a closed-loop system with the ERA 1101 computer and its associated converters as part of the loop.

Choice of sampling rate.-- Since the probability for error in a sampled-data system is decreased as the sampling rate is increased, it is desirable to make the sampling rate as high as the computer will allow. Since 30 microseconds are required to execute most computer instructions, it would be pointless to sample at a rate greater than this. Conversion speed is also a factor in choosing a sampling rate. In the discussion that follows, it is shown that a conversion rate of 500,000 bits per second is close to the upper limit for conversion speed. Thus, if an 11-bit input to the computer memory is considered to be the maximum length of digital data, 50,000 conversions per second is the maximum capability of the converter. Hence, the converter requires at least 20 microseconds to complete one conversion.

Any useful computer program requires many instructions to carry out a mathematical operation. The exact number of instructions will vary depending upon the operation, but a simple example will clarify what is involved. In order to add "A" to "B" and store the result, the computer must do the following:

1. Extract "A" from the memory and place "A" in a register.
2. Extract "B" from the memory and add "B" to "A", leaving the result in a register.
3. Store the result in the memory.

Each of these operations requires 30 microseconds, so the process of adding "A" to "B" and storing the result requires 90 microseconds. If real time computation involving an analog input-output scheme were involved, the following commands would be typical of those required to add two inputs resulting from samples taken at different times:

1. Command the converter to sample the input signal. (Sample "C")
2. Read the quantized sample into a computer register.
3. Store sample "C" in the memory.
4. Command the converter to sample the input signal. (Sample "D")
5. Read the quantized sample into a computer register.
6. Extract sample "C" from the memory and add "C" to "D", leaving the result in a register.
7. Command the converter to accept an output signal, and read out the results to the output converter.

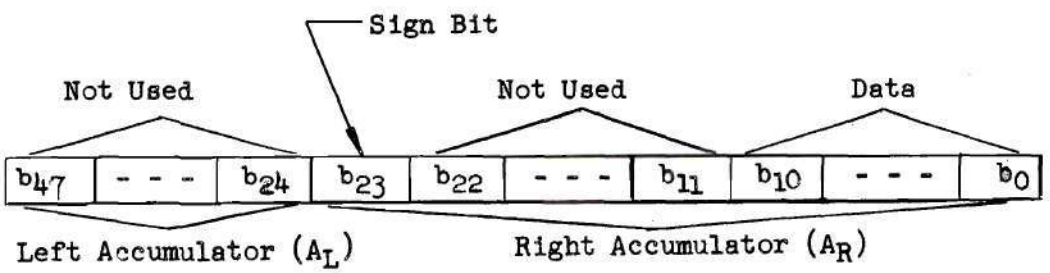
In this sequence, instructions one and four each require 20 microseconds for completion, while the others require 30 microseconds each. Thus, 80 microseconds elapse between the time of the beginning of sample "C" and the beginning of sample "D", while 110 microseconds elapse from the beginning of sample "D" until the conclusion of the read-out of the result.

This example makes apparent the necessity for having a variable sampling rate. In order to make the converter compatible with the mathematical operations being performed by the computer, it is essential for the sampling rate to be a variable controlled by the computer itself, with the 20 microseconds between samples set by conversion speed no longer being a limiting factor, since even the most simple program would require more computer time than this to carry out the operations involved. It is again emphasized that the maximum sampling rate is rigidly set by the complexity of the operations performed by the computer upon the input signal, and each system should be carefully analyzed using Laplace transform, Z-transform, or other applicable procedures to determine the effect sampling at the rate prescribed by the computer program will have upon it.

Quantizing.-- As mentioned previously, quantizing involves the conversion of a continuously varying signal, which may assume any of an infinite number of levels, into a representation which involves a finite number of levels. Since the process of quantizing is extremely non-linear by its very nature, it is quite difficult to evaluate the effect of quantization, even for linear systems. Impressive

mathematical analyses of quantization have been developed based upon the statistical approach. For example, it can be shown that little increase in accuracy is gained by increasing the number of significant bits beyond three when dealing with statistical operations (1). For the problem at hand, however, examples of this sort are of little use, since many of the problems which would be attacked are of a non-statistical nature. Precision is of extreme importance, and the smaller the quantizing level, the more accurate will be the representation of the true signal.

Choice of quantizing level.-- As mentioned previously, the Accumulator of the ERA 1101 computer is capable of accepting a 48-bit word. If the Accumulator were utilized as the input or output register for the converters, the following arrangement would be possible:



Of particular interest is the truncation that results from expressing an infinitely variable continuous function as a finite approximation. Consider the 11-bit binary representation above and note that the maximum truncation error ($E_{t\ max}$) approaches one part in 2047, or

$$E_{t\ max} = \frac{1}{2^{10} - 1} \times 100\% = 0.049\% \text{ of maximum.}$$

Also of some importance in the choice of a quantization level is the physical configuration of the converter. In order to take advantage of recent improvements in solid-state devices, it will be desirable to transistorize the converters. Hence, it is reasonable to assume that the maximum input voltage to the unit will be on the order of one volt. For an 11-bit converter with a maximum input of one volt, if all 11 bits are to be significant, the quantization level must be

$$E_q = \frac{1}{2047} = 488 \text{ microvolts.}$$

Codes.-- Invariably, the expression of information for use in a digital computer involves the use of codes. In this sense, a code is any unique arrangement of symbols for the expression of a quantity. To be of practical use, codes involve orderly arrangements of symbols and follow rigid rules for combinations of symbols and mathematical operations upon and with symbols. The most commonly known code makes use of the Arabic numerals 0 through 9 and follows the rules of decimal arithmetic. For every-day use, decimal numbers are universal, and a number such as 2379 leaves a specific idea of a quantity in the mind of the person who sees it. In reality, 2379 means $2 \times 10^3 + 3 \times 10^2 + 7 \times 10^1 + 9 \times 10^0$, but familiarity with decimal quantities leads the observer to skip the thought processes involved in this expression of a decimal number.

Since electronic devices are not particularly adaptable to the decimal system, which requires the expression of quantities involving ten different levels for each power of the base ten, codes involving fewer levels have been evolved for digital computation. The simplest

possible codes use two levels and have been given the name binary codes. The numerals 0 and 1 are used exclusively in the binary system, and each binary position receives the name "bit", just as each decimal position is called a digit.

A common binary code makes use of the same sort of positional notation as common decimal representation, i.e., the value of each successive bit differs by the base factor, which in this case is two. Thus, the binary number 1101 means $1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$, and the decimal equivalent is seen to be 13.

It follows that it is possible to express any integral number I by use of any integral number for the base. Hence,

$$I = a_n B^n + a_{n-1} B^{n-1} + \text{- - -} + a_2 B^2 + a_1 B^1 + a_0 B^0.$$

B stands for the base of the number system employed and equals the number of distinct levels involved. The a's may assume the integral values of any of the levels involved. Assume zero to be the smallest level so the largest level will have the value B - 1, then a_k $(0 \leq k \leq n)$ may assume any of the integral values between and including zero and B - 1.

Similarly, the general expression of a fraction F in any base is

$$F = a_{-1} B^{-1} + a_{-2} B^{-2} + a_{-3} B^{-3} + \text{- - -} + a_{-n} B^{-n}.$$

Bases which are frequently used are binary (base 2), octal (base 8),

decimal (base 10), and bi-octal (base 16).

Arithmetic operations are extremely simple in the binary system as shown by the addition and multiplication tables of Figure 7. Various binary codes other than the positional have been developed. Of particular interest in analog-to-digital conversion is the Gray code (8). This code has the advantage of having a single-bit change between successive numbers, and is of the form shown in Figure 8.

For the Gray code, the absolute value of a one in the jth column is given by

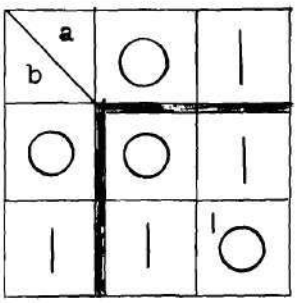
$$\sum_{i=0}^{i=j} 2^i.$$

This code has a sign associated with each position which is positive for all odd-numbered ones starting at the left and negative for all even-numbered ones. There exists a simple rule of thumb for translating to conventional binary code from Gray code (1):

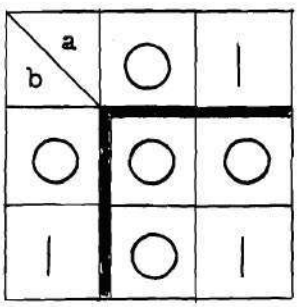
> Leave the most significant one unchanged. Complement each successive bit (change ones to zeros and zeros to ones) as many times as there are ones preceding it in the Gray-code number.

For example, the Gray-code number 1000 may be changed to conventional binary representation as follows:

1. The first one remains unchanged.
2. The first zero is complemented since a single one precedes it.
3. The second and third zeros are complemented.



a. Complete Binary Addition Table (a+b)



b. Complete Binary Multiplication Table (a x b)

Figure 7. Binary Arithmetic Tables

Decimal	Gray Code
0	0000
1	0001
2	0011
3	0010
4	0110
5	0111
6	0101
7	0100
8	1100
9	1101
10	1111

Figure 8. Gray Code Representation of the Decimal Numbers Through Ten

Thus, the conventional binary representation is 1111, which is equivalent to 15 in the decimal system.

Choice of a code.-- The ordinary binary code is representative of a class of codes called positional codes, while the Gray code is representative of a class called unit-distance codes. In order to use the Gray code with a machine such as the ERA 1101 computer, it would be necessary for the machine to first convert the Gray representation into ordinary binary form. This is because the ERA 1101 computer performs mathematical operations using standard binary arithmetic, while the Gray code does not follow standard binary rules. Since such conversions would require additional machine time, and since a converter using a unit-distance code would be more complicated in design, the standard binary code has been chosen for the converters to the used with the ERA 1101 computer.

CHAPTER IV

CODING TECHNIQUES

Comparison coding.-- Among the more sophisticated of electronic coding devices is a class of coders which compares the analog input voltage with an internally synthesized voltage. A switching circuit, which is an integral part of the coder, changes the internally synthesized voltage until it agrees with the input. The block diagram of a simple comparison coder is shown in Figure 9. In this circuit, the local voltage synthesizer is a decoder in which the internal sources are turned on or off by the control circuit. The control circuit turns on various combinations of sources until the decoder output and the voltage to be coded are in agreement. The state of the sources in the synthesizer (either "ON" or "OFF", i.e., zero or one) then form the quantized binary representation of the analog input.

Limiting factors in the choice of components for each of the major blocks of the comparison coder are accuracy and speed of conversion. The former is significant in the comparison and decoding circuits, while the latter predominates for the control circuit. Examination of several types of possible control circuits reveals various approaches to the problem of conversion time. A servomechanism approach may be followed in which the comparison circuit would be designed to indicate a positive, negative, or zero difference between the analog input and the synthesized decoder output. If a

difference exists, the states of the decoder circuits are then changed until the input and output agree. Here the limiting factor in conversion time is the decoder, which must respond rapidly enough to follow the dynamics of the input.

Another possibility utilizes the control circuit to turn on the decoder sources in the following sequence:

b_0

b_1

b_0 and b_1

b_2

b_0 and b_2

b_1 and b_2

b_0, b_1, and b_2

.
.
.

b_0, b_1, b_2, . . . , b_n

Here, b_0 designates the least significant bit and b_n the most significant. To generate an n-bit number would require $2^n - 1$ counts. For an 11-bit output with the control circuit switching at a rate of 5×10^6 times per second, the maximum conversion time would be

$$\frac{2047 \text{ counts}}{5 \times 10^6 \text{ counts/second}} = 410 \text{ microseconds.}$$

This is an unreasonable conversion time and this type of coder will not be considered for the converters.

Comparison coding with cascaded stages.-- The limitations on conversion time are theoretically eliminated in a unique circuit devised by B. D. Smith (9). The essential components of his circuit are shown in the block diagram of Figure 10. This scheme derives a b-bit number by utilizing b single-bit stages in cascade. Each stage uses a comparison circuit and a subtracter. The comparison circuit is designed to have an output which is either zero or equal to the stage reference voltage. The latter appears at the output only when the input is equal to or greater than the reference level. A circuit which will perform this function is the familiar Schmitt trigger circuit. In order to minimize error, it would be essential to have a Schmitt trigger circuit with essentially zero hysteresis. In general, this is not physically realizable if vacuum tubes are employed, since interelectrode capacitance would tend to cause a steady-state limit cycle of finite amplitude at the switching point. Solid state devices have smaller interelectrode capacitances, however, and an acceptable zero-hysteresis Schmitt trigger circuit which was successfully tested in the laboratory is described in Appendix A.

Return to the description of the cascaded stage comparison coder and note that the output of the Schmitt trigger circuit is subtracted from the continuous input. The resulting signal, which is equal to $V_{in} - V_{ref}$, is fed to the next stage. If the least significant bit (the quantization level) is produced by q_n volts, the reference level of each other stage is given by $2^{n-k}q_n$ volts. Here n is the number of stages, k is the stage of interest, and k = 1 is the most significant stage. Especially for a transistorized

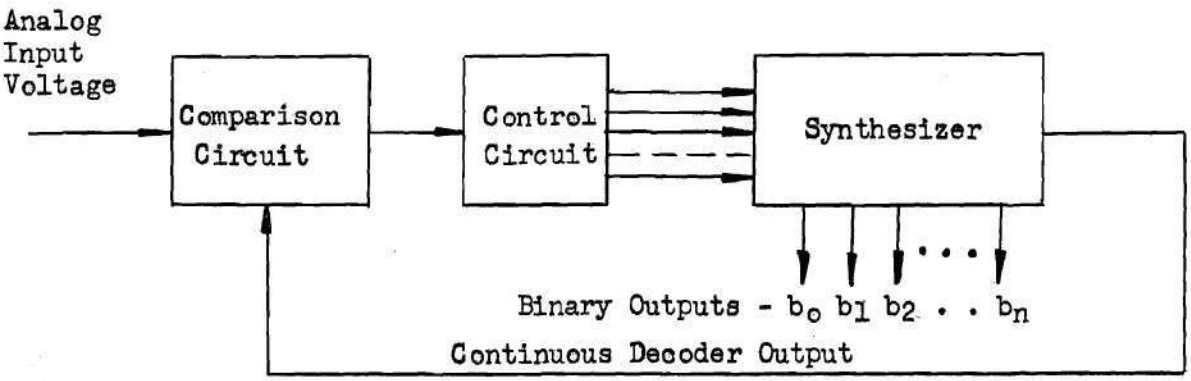


Figure 9. Comparison Coder Block Diagram

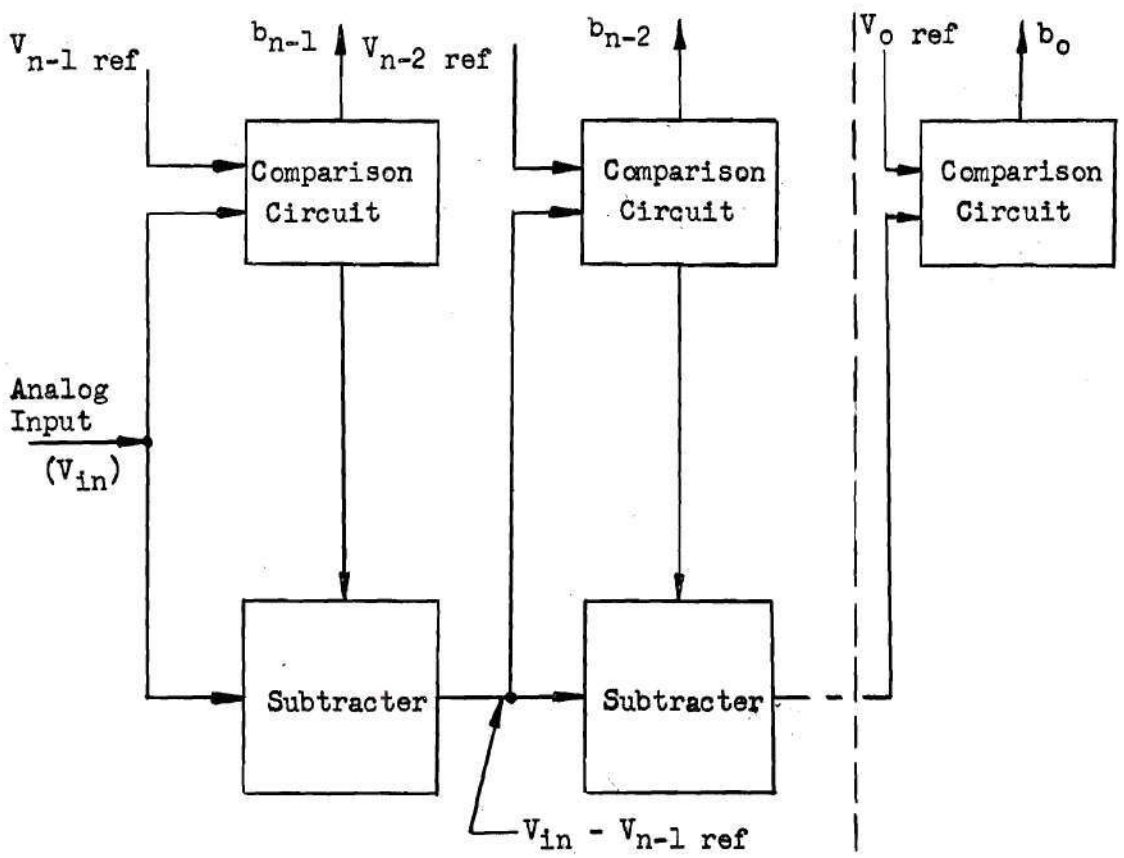


Figure 10. Comparison Coder With Cascaded Stages

device, this scheme quickly gets out of hand. For example, suppose $q_n = 1$ and a ten stage quantizer is desired. The reference level of the most significant stage would then have to be

$$2^{10-1}(1) = 512 \text{ volts},$$

a value which would be unreasonable even for vacuum tubes!

More reasonable results are obtainable from a slight modification of the above ideas. All reference voltages may be made the same if the output of each subtracter is multiplied by two. This reference is then $2^{n-1}q_n$ volts, where n is the number of stages and q_n is the quantization level. Unfortunately, this scheme has the disadvantage of multiplying the error by two in each stage also, which means that accurate multipliers and subtracters must be used.

This problem of accuracy may be met by utilizing a tool commonly used in analog computation -- the operational amplifier. The block diagram of a typical operational amplifier is given in Figure 11. The transfer function for this circuit may be expressed as

$$\frac{V_o}{V_i} = \frac{A}{1 + FA} = \frac{1}{F + \frac{1}{A}} .$$

If $A \rightarrow \infty$, $\frac{V_o}{V_i} \rightarrow \frac{1}{F}$, and the accuracy of the output is dependent only on the feedback element and the input signal, if drift is negligible. Several operational amplifiers meeting these requirements are on the market and may be utilized to give accuracies within 0.005 per cent of the maximum input (10).

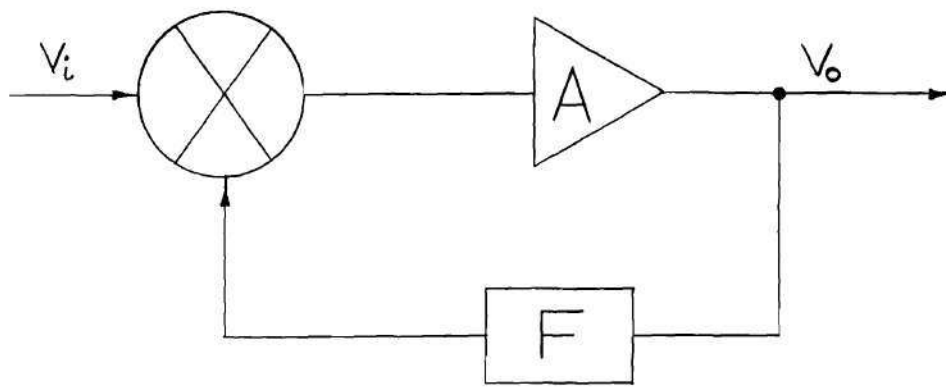


Figure 11. Operational Amplifier Block Diagram

An example will clarify the functioning of a cascaded stage comparison coder having a single reference voltage. Suppose it is desired to convert to binary a voltage between 0.00 and 15.99 volts in magnitude. This may be accomplished in a 12-bit register of the form previously described. If we consider the case of a four-bit binary representation of the whole numbers $0 \leq n < 16$ quantized to one volt, the reference voltage would be

$$V_R = 2^{4-1} = 8 \text{ volts.}$$

This approach may be extended to the fractional bits as well, and the resultant outputs are shown in Table 1 for an input of +12.99 volts.

Limiting factors in conversion time are the time required for each Schmitt trigger circuit to trigger and the response time of the operational amplifiers in cascade. Less than one microsecond per stage is a reasonable response time for the Schmitt trigger circuits and operational amplifiers with a response of 0.5 microsecond per stage have been built (11). This means that a total conversion time of less than 20 microseconds could be expected for an 11-bit representation. Such amplifiers are expensive and difficult to maintain in proper operating condition, however, and since an 11-bit converter would require 11 of these in cascade, this choice for a converter design is discarded.

Comparison coding by successive approximation.-- The block diagram of an alternative approach which also makes use of servomechanism

Table 1. Cascaded-Stage Coder Voltages

Stage	Input Voltage	Output Voltage	Bit	Weight
Sign	12.99	12.99	0	(plus)
1	12.99	2(12.99 - 8.00) = 9.98	1	2^3
2	9.98	2(9.98 - 8.00) = 3.96	1	2^2
3	3.96	2(3.96 - 0.00) = 7.92	0	2^1
4	7.92	2(7.92 - 0.00) =15.84	0	2^0
5	15.84	2(15.84 - 8.00) =15.68	1	2^{-1}
6	15.68	2(15.68 - 8.00) =15.36	1	2^{-2}
7	15.36	2(15.36 - 8.00) =14.72	1	2^{-3}
8	14.72	2(14.72 - 8.00) =13.44	1	2^{-4}
9	13.44	2(13.44 - 8.00) =10.88	1	2^{-5}
10	10.88	2(10.88 - 8.00) = 5.76	1	2^{-6}
11	5.76	2(5.76 - 0.00) =11.52	0	2^{-7}

methods for comparison coding is shown in Figure 12. An analog input voltage is applied to the comparator. If the input from the summing and weighting network exceeds this input, a pulse is generated by the comparator and applied to the control circuits. The control circuits are of such a nature that the count contained in the output register of the decoding network is changed one bit at a time, starting with the most significant bit, until the comparator indicates that no further error exists. The summing and weighting networks are the keys to the success of this scheme, and an example serves to illustrate the techniques involved more clearly.

The outputs of the summing and weighting network are given the following weights:

$$V_k = V_{k-1} + \frac{1}{2^{k-1}} V_o.$$

Here V_k is the sum total of the contributions of all sources through the kth, V_{k-1} is the sum total of the contributions of all sources through the (k-1)st, V_o is the weight of the most significant source, and n is the total number of significant bits. Note that V_o must equal 2^{n-1} for a binary read-out. Thus, the expression for V_k becomes

$$V_k = V_{k-1} + 2^{n-k} .$$

If V_k is greater than the analog input voltage, then the kth bit, b_k, is a zero and the kth stage adds no contribution to the total summed output of the k weighted stages. If V_k is less than or equal to the analog input, b_k is a one and the kth stage adds a

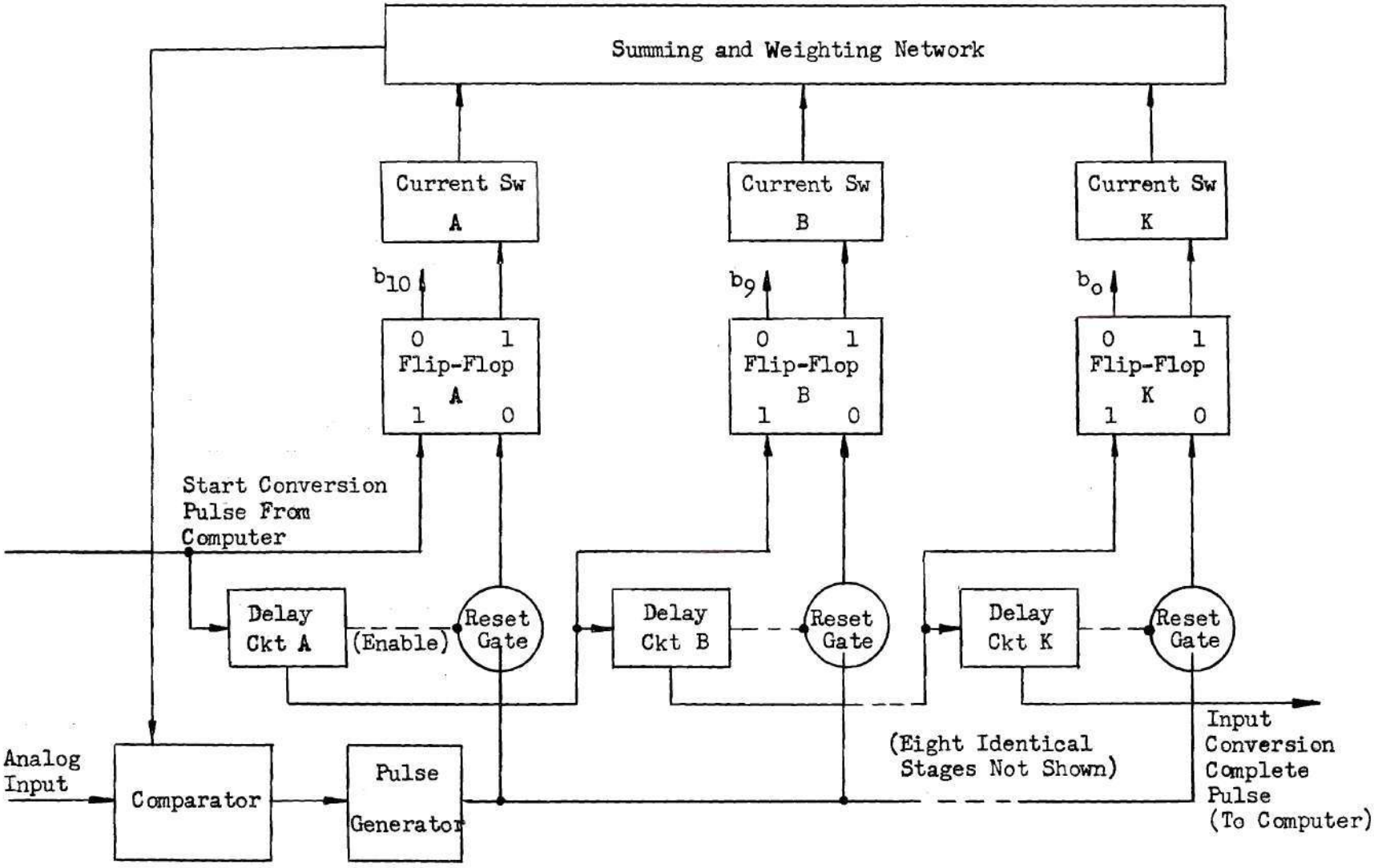


Figure 12. Successive Approximation Comparison Coding

contribution of $2^{(n-k)}$ volts to the previous stage outputs. Assume a five-bit register and an input of 26 volts. The voltages at each stage may be tabulated as shown in Table 2. Note that the binary representation for decimal 26 is indeed 11010. Hence, this scheme gives the correct representation of the analog input in binary form.

Table 2. Stage Voltages in Successive-Approximation Coder

Stage	V_{k-1}	+ 2^{n-k}	= V_k	Is this greater than 26 volts?	b_k
1	0	16	16	no	1
2	16	8	24	no	1
3	24	4	28	yes	0
4	24	2	26	no	1
5	26	1	27	yes	0

The successive-approximation approach requires a maximum of one change of state for each stage. If it is assumed that one microsecond per change of state is a reasonable time, a maximum of 11 microseconds would be required for these transitions in an 11-bit register. Additional delays might be introduced by the control circuits and comparator, but if these delays can be made small, this type of coder promises to meet the conversion time requirements previously established.

An examination of the problem of accuracy is in order at this point. For the last bit to be significant, the comparator must be able to distinguish between an analog input and an input from the summing and weighting network which differ by no more than the value of that bit. Thus, for an 11-bit representation, the comparator must be able to detect a difference between the continuous input and the summing and weighting input as small as one part in 2047. Differential amplifiers have been developed which are capable of accuracy much better than this (12).

The other major source of error is the summing and weighting network of the decoder. A typical example of a network used for decoding binary numbers is shown in Figure 13 (1). When the kth bit is <u>one</u>, switch S_k is closed and current source T_k adds a proportional amount to the output voltage V_o. If the kth bit is a <u>zero</u>, switch S_k is open and current source T_k adds no contribution to the output. All current sources T_o to T_n are of equal magnitude I, and are assumed to have infinite impedance. Therefore, T_k is not affected by the presence or absence of other sources when S_k is closed and the only loading on T_k is that represented by the resistive network consisting of R and 2R. The nature of the circuit is such that the load on every interior stage is 2R looking to the left of the kth node, 2R looking to the right, and 2R looking up. Thus, the total load R_k on every interior stage is given by the relation

$$\frac{1}{R_k} = \frac{1}{2R} + \frac{1}{2R} + \frac{1}{2R} = \frac{3}{2R}$$

or,

$$R_k = \frac{2R}{3}.$$

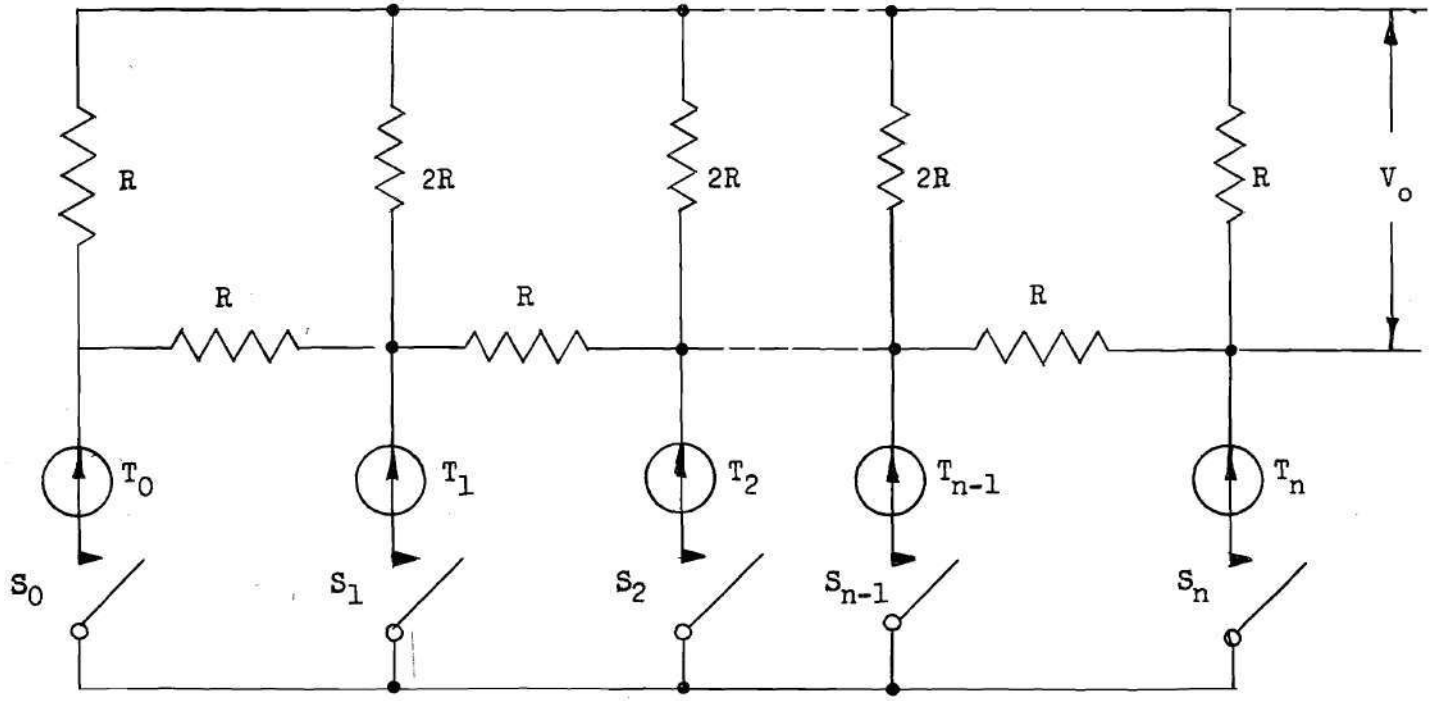


Figure 13. Binary Digital-to-Analog Voltage Synthesizing Network

Note that the load on the end stages is also $\frac{2}{3}$ R, so each stage has the same load.

Since each current source sees the same load and all sources are of the same magnitude (i.e., $I_k = I$), it follows that each source sets up a voltage $E_k = \frac{2}{3}$ RI between its node and ground. Because of the arrangement of resistance values in the ladder network, a voltage E_k at node k is attenuated by a factor of two at the (k+1)st node, by a factor of four at the (k+2)nd node, etc. The total output voltage is seen to be

$$V_o = \frac{E_o}{2^n} + \frac{E_1}{2^{n-1}} + \cdots + \frac{E_n}{2^o} .$$

The binary number to be decoded may be expressed in terms of powers of two

$$b = a_n 2^n + a_{n-1} 2^{n-1} + \cdots + a_1 2^1 + a_o 2^o$$

where a_k is either zero or one.

Hence, the voltage contributed to the output by the kth stage may be re-expressed as

$$E_k = \frac{2}{3} \text{RI} \frac{a_k}{2^{n-k}}$$

and the output voltage is

$$V_o = \frac{2}{3} \text{RI} \left(\frac{a_o}{2^n} + \frac{a_1}{2^{n-1}} + \cdots + \frac{a_{n-1}}{2^1} + \frac{a_n}{2^o} \right),$$

or $$V_o = \frac{2}{3} RI \left(a_o 2^o + a_1 2^1 + \cdots + a_{n-1} 2^{n-1} + a_n 2^n\right)$$

and $$V_o = \frac{2}{3} RI \frac{b}{2^n} .$$

Hence, the output voltage is a linear function of the binary number to be decoded, and it is seen that the limits on accuracy are imposed exclusively by the current sources and the resistors. Resistors with guaranteed errors less than 0.01 per cent are commercially available. Thus, (except for the constant of proportionality), with ideal current sources assumed, this is the maximum error which would be introduced at the most significant node. All nodes combined could introduce a total error no greater than this, so the maximum possible error for a resistive ladder network of this sort should be less than 0.01 per cent of the maximum input.

By nature, a transistor in the common base configuration is a close approximation to the ideal current source, and should supply a constant current within 0.05 per cent for this network. Thus, the total error introduced by this decoding network is less than 0.1 per cent of the true input.

In summary, the comparison coder using successive approximations meets the requirements for speed of conversion and accuracy necessary in the converters to be used in conjunction with the ERA 1101 computer. While it will be necessary to use expensive components in the comparator network in order to gain the desired conversion speed and accuracy, this network is used only once, regardless of the total number of significant bits involved. This type of converter should be much less expensive to

build and easier to maintain than the cascaded-stage converter previously described. In addition, the decoder circuit is immediately adaptable for use as a digital-to-analog converter, which will also be required in the total system used with the computer.

For these reasons, this type of coder is chosen for the basic design to be used in the input and output converters for the ERA 1101 computer.

CHAPTER V

DESIGN OF THE ANALOG-TO-DIGITAL CONVERTER

System description.-- The block diagram of an analog-to-digital converter employing successive-approximation techniques is shown in Figure 12. Circuits to implement this scheme have been developed by William B. Towles (13). Towles' circuit, which was conceived in 1957, had a conversion capability of 200,000 bits per second and an accuracy of 0.5 per cent of the full-value input of five volts. By utilizing more recent solid-state components it should be possible to increase the conversion capabilities of this unit to well over 500,000 bits per second with an accuracy better than 0.1 per cent of full-value input.

Upon receiving an initiate pulse from the digital computer, the most significant bit in the converter register is driven from the zero to the one condition. Simultaneously, delay circuit A is triggered and applies an enabling pulse to reset gate A. The current switch and summing and weighting networks form a current-switch decoder of the type previously described. Since the most significant bit is now in the one position, a voltage proportional to the significance of that bit appears at the comparator input. If the weighted voltage exceeds the analog input signal to the comparator, a pulse is generated by the comparator which is applied to all of the reset gates. Since only reset gate A has been enabled, the pulse passes through this gate and resets flip-flop A to the zero condition. Conversely, if the weighted

input to the comparator does not exceed the analog input, no reset pulse is generated, and the most significant stage remains in the one position.

In order to continue the same sequence of operations in stage B, the trailing edge of the enabling pulse of delay circuit A is differentiated. This produces a new initiate pulse which is then applied to stage B. The comparator action continues through all 11 significant stages, as outlined in the previous discussion on successive-approximation comparator circuits.

Compatibility with the ERA 1101 computer.-- The successive-approximation comparison coder described in this section is readily adaptable for use with the ERA 1101 computer. Conversion action is started by an initiate pulse from the computer. The origin of this pulse will be discussed more fully in the chapter on modification of existing computer circuits; so, for the present, it is sufficient to assume the existence of such a pulse. Upon completion of the conversion, a pulse may be derived from the trailing edge of the final stage delay circuit and sent to the computer to initiate storage of the quantized data in the machine memory.

Recall that the operating structure of the ERA 1101 computer is such that the complement of a number must be sent to the Accumulator in order for the number itself to appear in this register, since it is subtractive in nature. Likewise, the results of a computation which appear in the Accumulator are in the one's complement representation. This places no limitation upon the output converter,

however, since either the converted number or its complement may be obtained from the flip-flop register which controls the summing and weighting network. This follows from the nature of a flip-flop, which always has two output points. One output is zero and the other one at any given time. Hence, the problem of obtaining the complement of the quantized data is solved by connecting the output leads to the complementary outputs of the individual flip-flops.

It is necessary to choose a computer register for the removal of data from the machine at this time. Since the Accumulator is the most versatile machine register, this is the register chosen. The results of a computation will appear in the 11 right-most bits of the right Accumulator (A_R). The remaining 13 bits of A_R will be the same as the sign bit, which is the left-most bit of A_R. Upon completion of a computation, a pulse will be sent to the input converter to initiate quantization of the analog signal at the instant of interest. At the same time, the contents of the Accumulator will be parallel-fed into the register of the output digital-to-analog converter.

Upon completion of the input conversion, a pulse will be sent to the computer from the input converter to initiate memory storage of the input data. The same pulse will remove the output converter from the circuit to prevent the inadvertent transmission of input data to the output. The converter will then parallel-feed the input data to the 11 right-most bits of the Storage Insertion Register, and the computer will store the 11 bits of input data and the associated 13 sign bits in the programmed memory location. A "resume computation" pulse is generated by the computer upon completion of storage.

This pulse will be utilized to clear the input converter.

In summary, data will be read into and out of the computer in the following sequence:

1. a. A pulse from the computer initiates analog-to-digital conversion in the input converter.

b. The same pulse clears the digital-to-analog output converter and initiates output conversion. At this instant, parallel-output data is read from the 11 right-most bits of the right Accumulator into the output converter register.

2. a. A pulse from the input converter informs the computer of the completion of input conversion and initiates parallel memory storage of the converted data.

b. The same pulse deactivates the output gates.

3. Upon completion of storage, the computer resumes computation and clears the input converter.

Comparator.-- As discussed previously, a good differential amplifier is the most important part of the comparator. The design procedure for such amplifiers has been extensively treated in the literature, and will not be repeated here (14). Low collector current is a desirable feature of such a circuit as is a well-matched, high-gain transistor pair. If fast conversion is to be accomplished, a high-speed switching transistor meeting these specifications should be chosen. The circuit of Figure 14 is typical of a comparator circuit which should meet the design requirements.

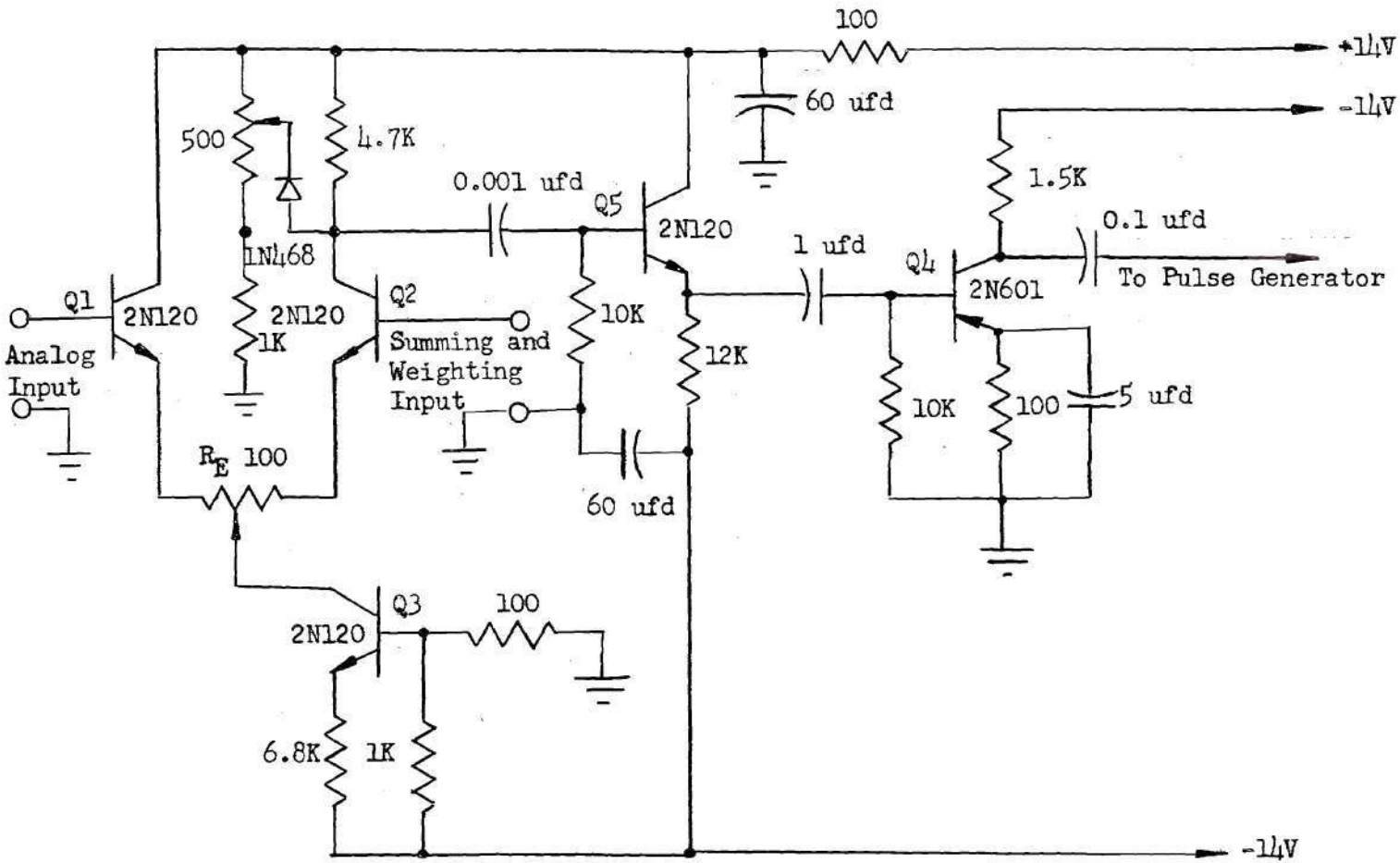


Figure 14. Comparator Circuit

Q1 and Q2 form an emitter-coupled difference amplifier with Q3 acting as a constant-current source to minimize common-mode effects at the output. The output at the collector of Q2 is clamped to a maximum value by a diode-voltage divider combination to minimize effects from power supply variations. R_E is placed in the emitter circuits to provide balance for emitter currents. When a "start conversion" pulse from the computer sets the first flip-flop, a sudden change in voltage appears at the collector of Q2 if the summing and weighting network output is greater than the analog input. As conversion pulses are generated in all succeeding stages and weighting sources are turned on, additional changes in voltage appear at the collector of Q2. Thus, when the input from the summing and weighting network exceeds the analog input, a negative-going pulse appears at the collector of Q2. This pulse must then be amplified if it is to be used to drive the flip-flops of the output register. A circuit which should accomplish the necessary amplification and provide a one-microsecond-wide pulse at the output is shown in Figure 15.

The transistors chosen for this circuit were not available for build-up of a demonstration model. However, transistors with all characteristics similar except switching time were available and were used in a laboratory set-up to demonstrate the sensitivity of the differential amplifier. The circuit used and a brief description of the test are given in Appendix B. The design characteristics of the transistor used in the test, the 2N342, are poorer than or equal to the 2N120 in every case. Hence, it can be concluded that the 2N120 will give equal or better results. A switching rate limiting factor is the blocking oscillator circuit. The circuit shown has a pulse width of

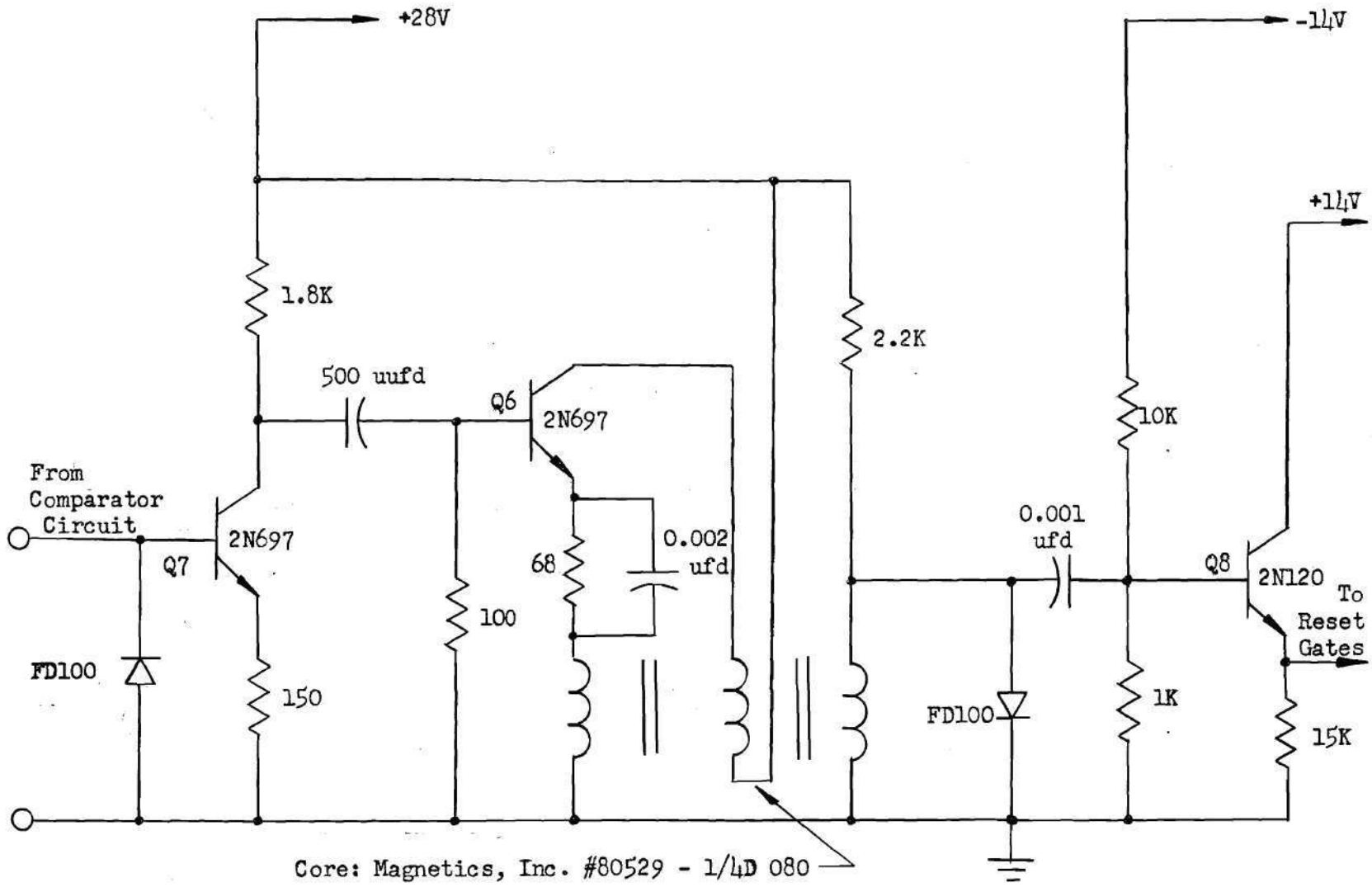


Figure 15. Reset Gate Pulse Generator

one microsecond. Hence, a reasonable upper limit on switching rate in the comparator will be on the order of 750,000 to 1,000,000 pulses per second.

Register.-- The output register consists of 11 identical circuits. The circuit for a single bit output is shown in Figure 16. Note that the initiate pulse from the computer pulses the delay circuit (a monostable multivibrator consisting of transistors Q10 and Q11) and sets the output flip-flop to the one condition. This pulse cuts off Q10 and turns on Q11 for a period of time determined by C4, R2, and R3. These values have been chosen to provide a pulse width of two microseconds. Since Q10 is cut off, its collector is sufficiently negative to bias the reset gate transistor Q12 such that an incoming pulse from the comparator circuit would be passed. If this positive pulse is coupled through C5 from the comparator card, the register flip-flop is driven back to the zero condition. This causes Q14 of the flip-flop pair to be cut off, which then cuts off Q18, causing a weighting voltage to appear at the output of the summing and weighting network, as will be described later.

At the conclusion of two microseconds, Q10 is again cut on, which couples an initiate pulse to the delay circuit and flip-flop bit register of the next less significant stage. This action is repeated for each significant bit until conversion is complete.

In order to assure fast switching, it is essential to avoid saturation of the delay circuit transistors. This is accomplished by clamping Q10 and Q11 to ground through suitable diodes as shown.

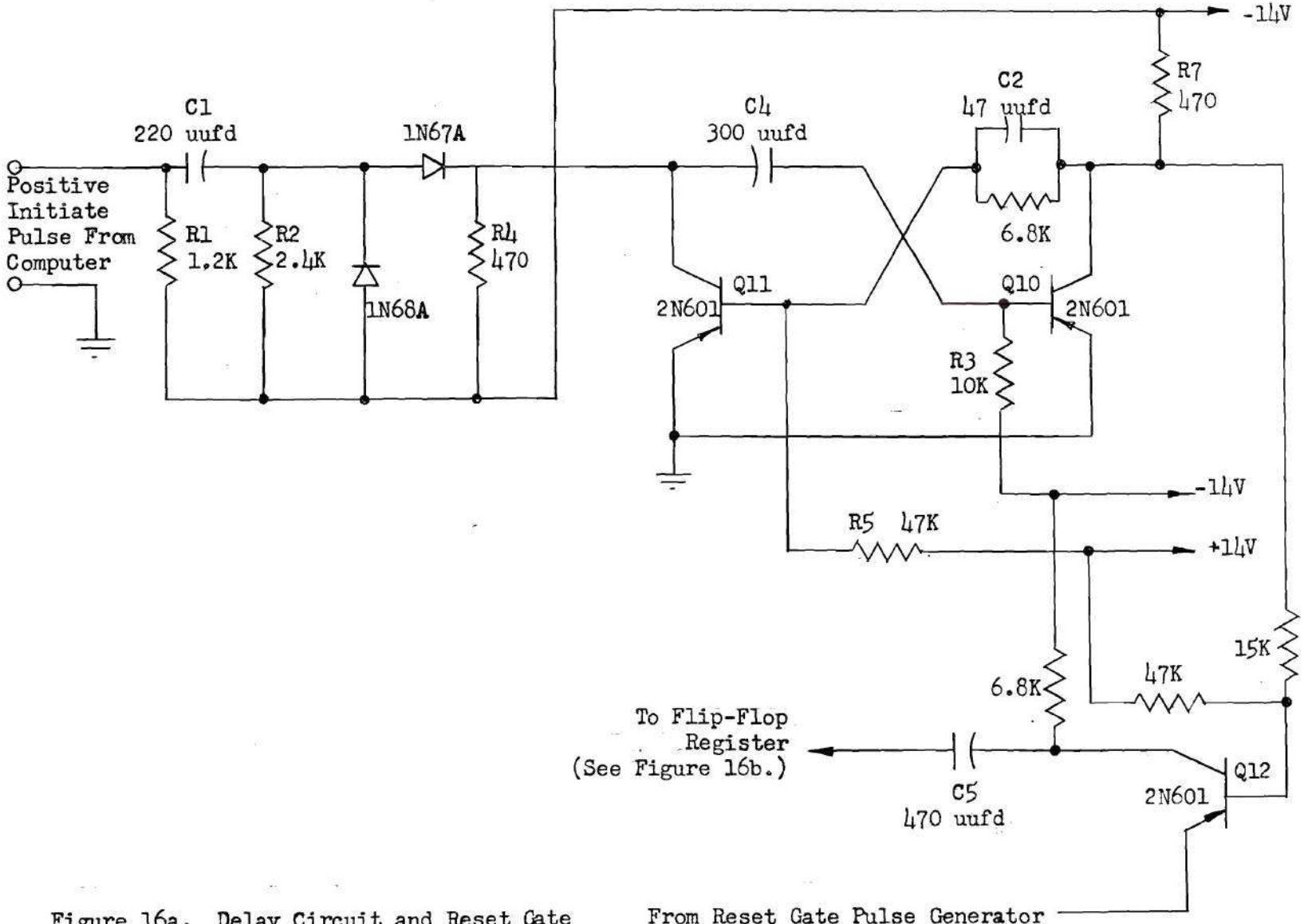


Figure 16a. Delay Circuit and Reset Gate

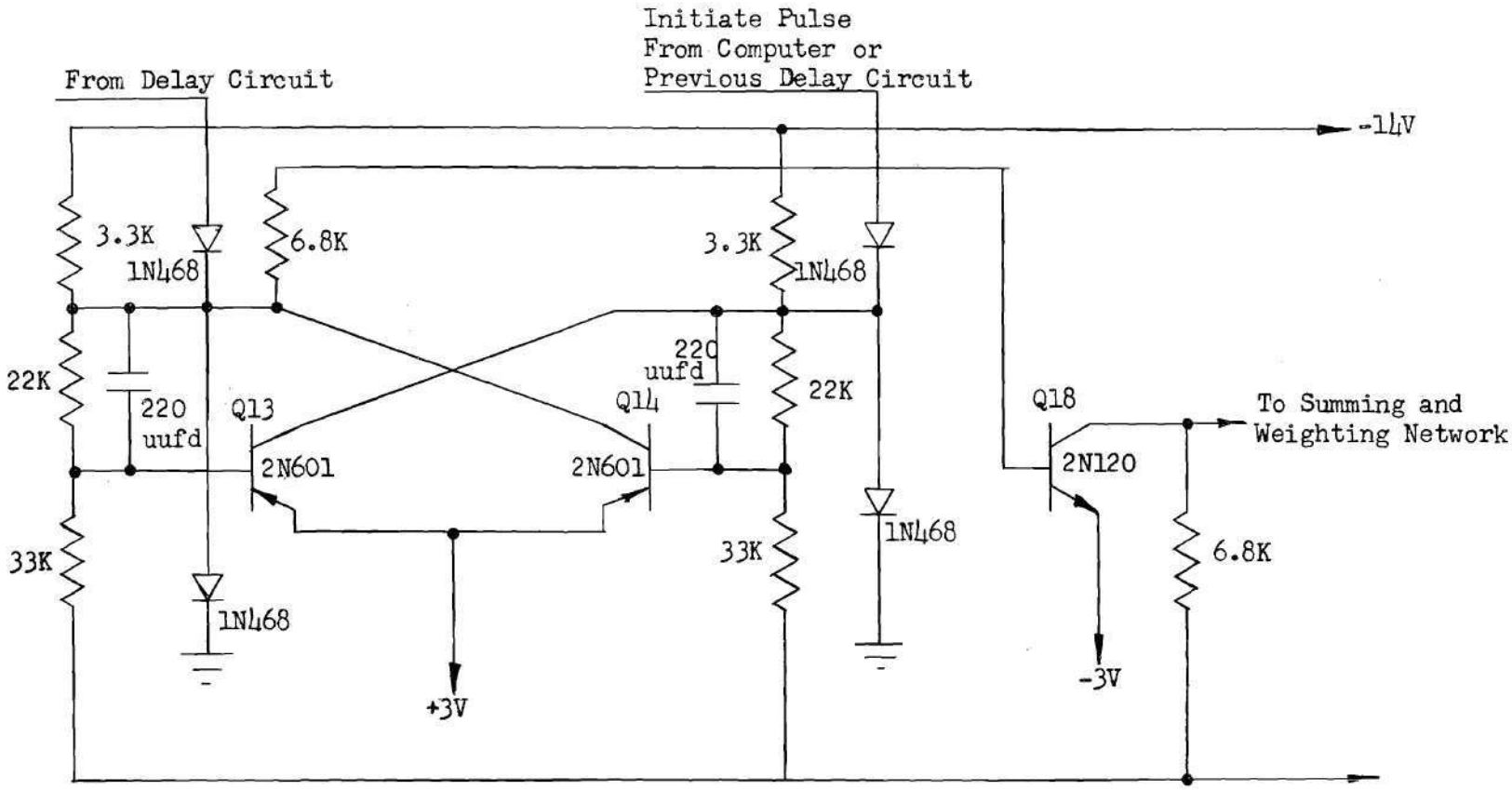


Figure 16b. Output Register and Current Switch

Summing and weighting network.-- Little has been said regarding the limitations placed on conversion speed by the comparator and output register circuits. This is because the primary limitation on conversion speed is the summing and weighting network. In the circuit shown in Figure 17, gating diodes with fast recovery time and high back resistance must be chosen in order to assure maximum switching speed and minimum error caused by reverse leakage currents in the resistive ladder. The SG1691 diode has a reverse current of only 0.25 microampere with 60 volts applied in the reverse direction. It also has a recovery time of approximately 0.5 microsecond.

The combination of this fast-recovery diode and a high-speed switching transistor, such as the 2N601, should guarantee a switching time in the summing and weighting network of less than two microseconds per bit. Thus, the determining factor in conversion time becomes the two microsecond pulse width of the monostable multivibrators used to drive the output-register flip-flops.

The purpose of R_C is to provide an adjustment for the current flowing in the constant-current sources. With -14 volts applied to the clamping diode (D_7, D_9, etc.) of a particular stage, the current flowing through the associated resistor in the ladder network (R_4, R_6, etc.) should be precisely 500.0 microamperes.

When the flip-flop output register associated with each stage of the summing and weighting network is in the one condition, the output current switch of that bit register is cut off and has approximately -14 volts at the collector. This voltage is applied to the clamping

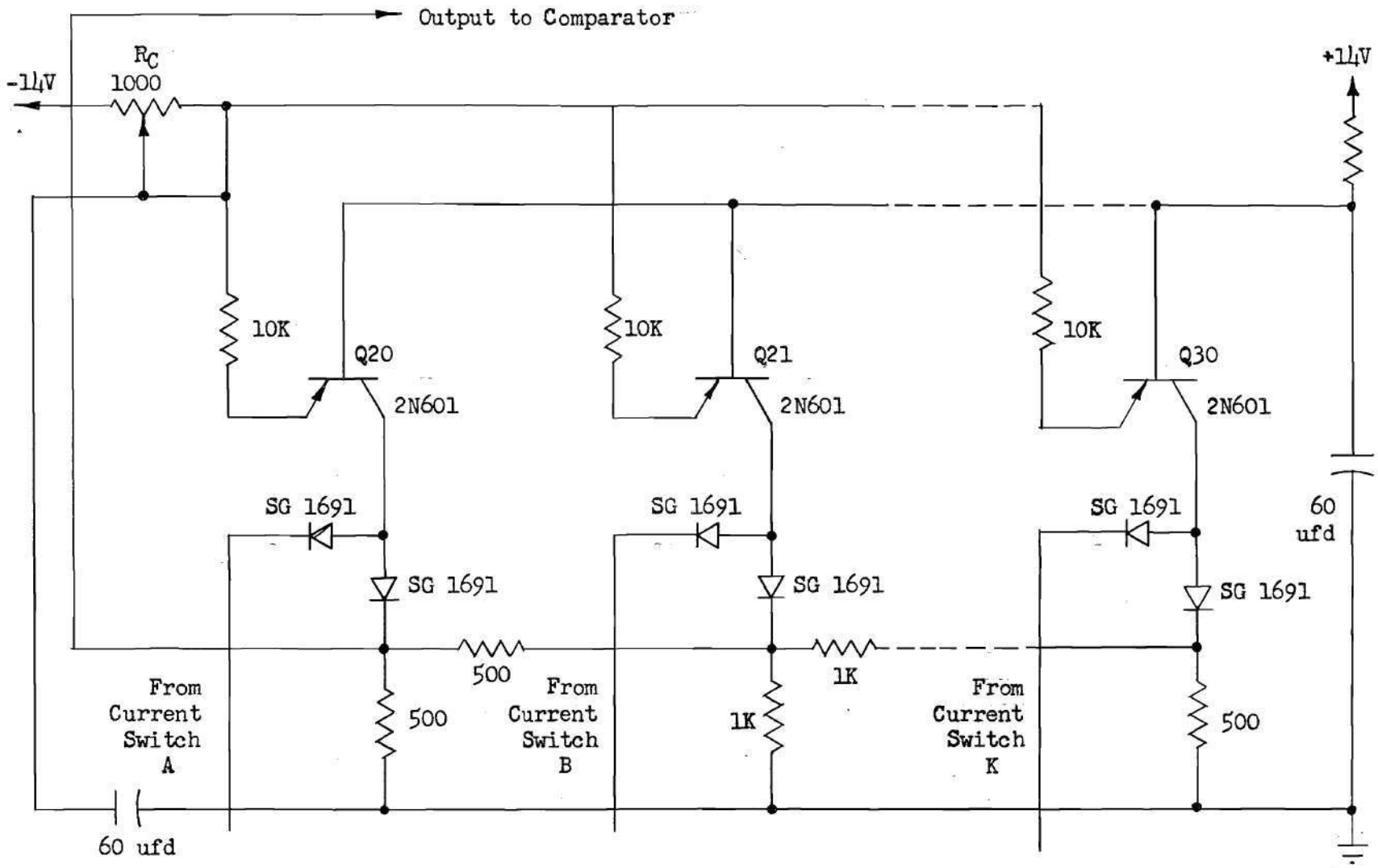


Figure 17. Summing and Weighting Network

diode of the current switch, which causes a current of 0.5 milliampere to flow in the collector circuit of the current source transistors (Q19, Q20, etc.) This current contributes a proportional voltage to the output of the summing and weighting network, which appears across R_4. Table 3 shows the voltage contributed to the output by a <u>one</u> in each binary position of the output register.

Table 3. Output Register Weights

Significance	2^{10}	2^9	2^8	2^7	2^6	2^5
Voltage Contribution (millivolts)	500.00	250.00	125.00	62.50	31.25	15.63
Significance	2^4	2^3	2^2	2^1	2^0	
Voltage Contribution (millivolts)	7.81	3.91	1.95	0.98	0.49	

Note that the summing and weighting network is designed to synthesize outputs for binary inputs representing all voltages between 0.0000 and 1.0000 ± 0.0005 volts. This is to ensure compatibility with the analog input to the comparator, which is limited to a maximum input of one volt.

<u>Digital-to-Analog conversion</u>.-- The output digital-to-analog converter may be constructed from bit registers and a summing and weighting network identical to those of the input converter. A block diagram of this scheme is shown in Figure 18. All that has been said concerning conversion time and accuracy for the input converter is also true for the output converter.

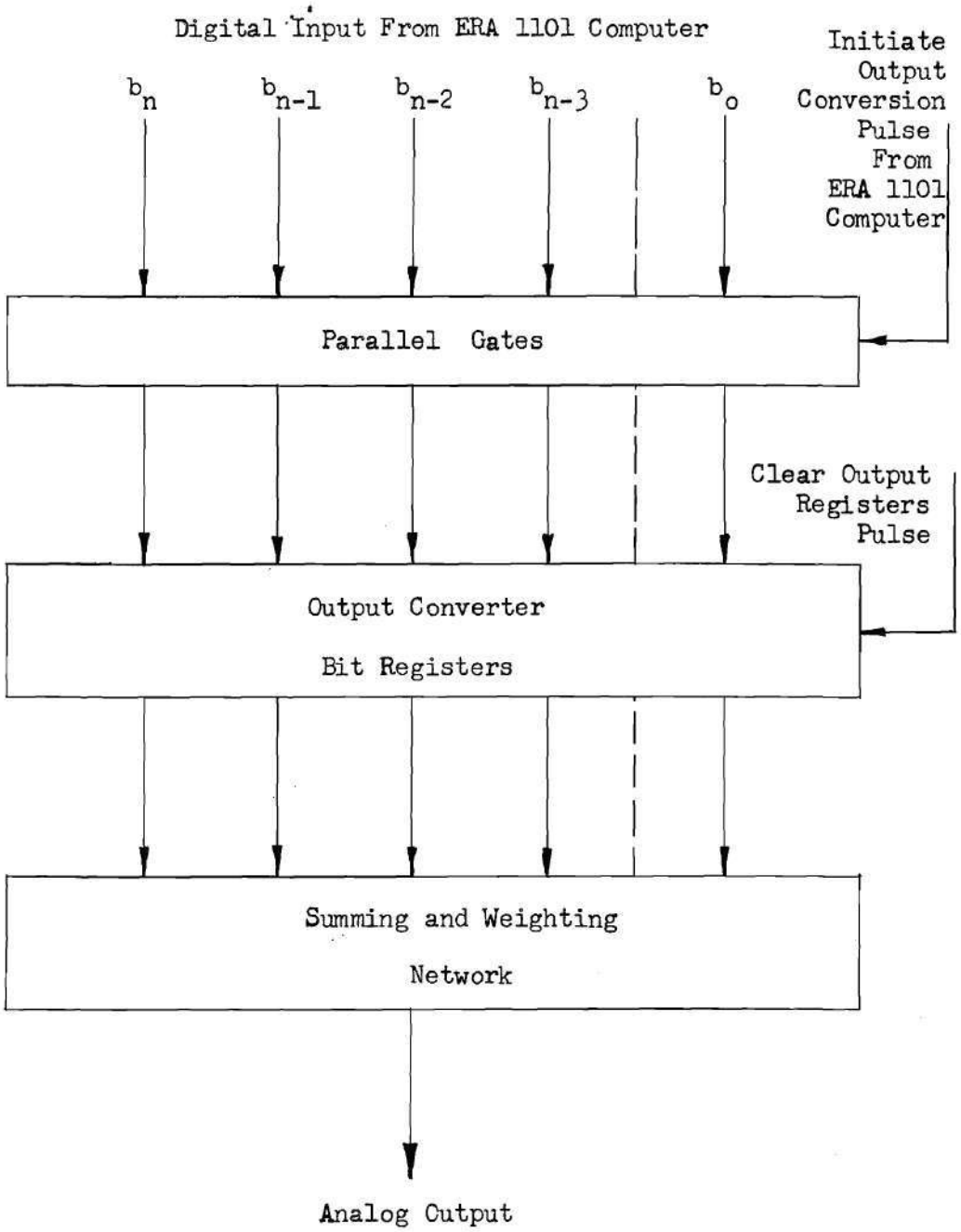


Figure 18. Output Digital-to-Analog Converter

CHAPTER VI

CONTROL CIRCUITS

System description.-- In order to accomplish input and output conversions at the proper times, several control circuits must be added between the present ERA 1101 computer circuits and the input and output converters. A block diagram of the necessary additions is shown in Figure 19. Note that existing amplifiers and gates are shown in phantom on this diagram.

Functioning of the control circuits.-- When the Command Translator Switch recognizes the programmed command "76", a signal appears at the input to gate G1 from the computer. G1 produces a pulse as soon as an enabling pulse appears on operation pulse distributor line number two (OPD #2) within the computer. Thus, G1 will allow the computer to stop only at the proper time in the operations sequence, which is at the conclusion of the operations initiated by the second operation pulse. When this pulse appears at the output of G1, it is applied simultaneously to the "computer stop" flip-flop (FF-A), the "read-out" flip-flop (FF-B), all 12 output bits, and the input analog-to-digital converter. The "computer stop" flip-flop is driven to the opposite state. This removes the enabling signal from the "computer stop" gate (G2), which interrupts the flow of clock pulses to the computer, causing all computer activity to stop.

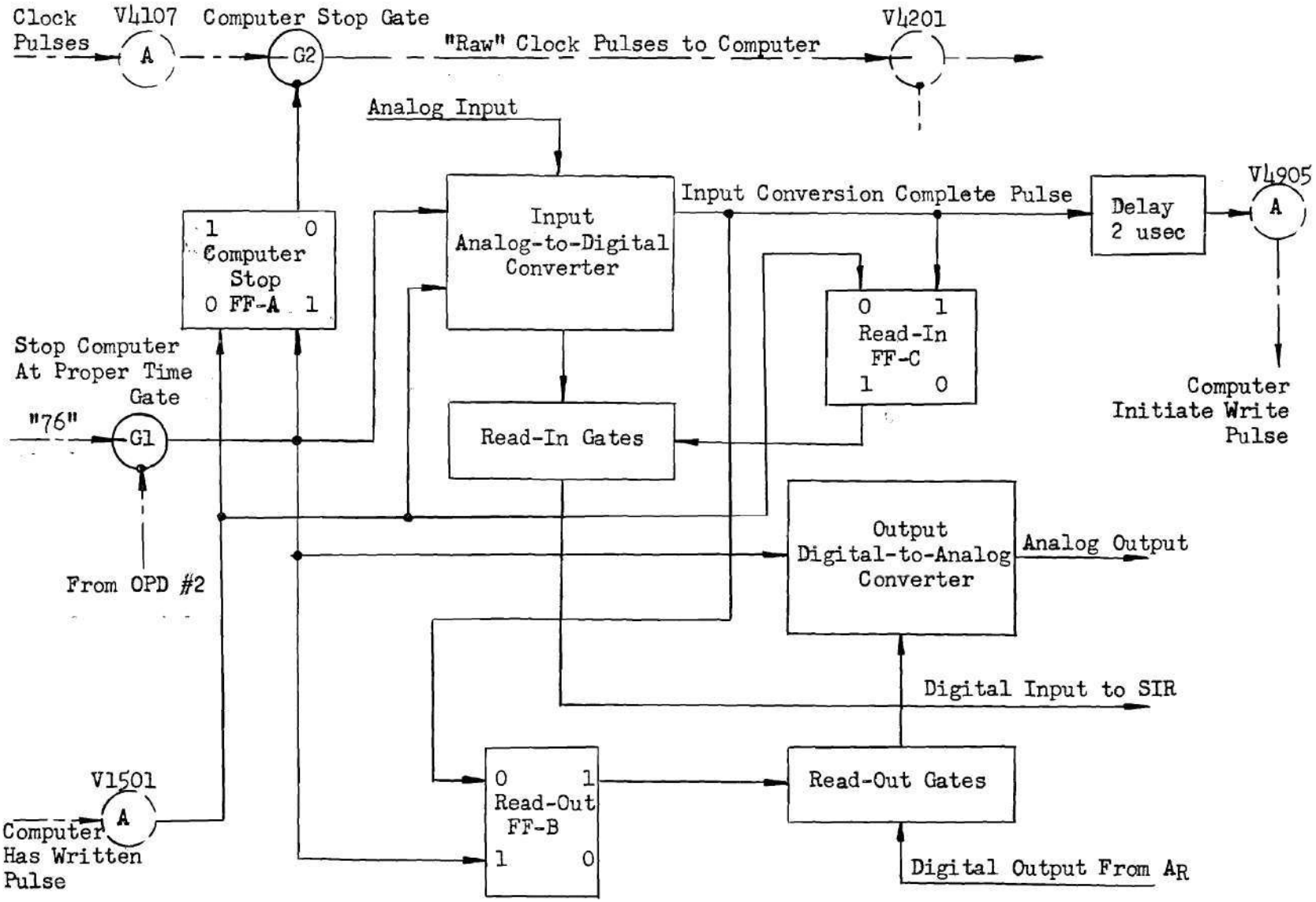


Figure 19. Control Circuits Block Diagram

All twelve bits of the output register are driven to the zero state by applying the pulse from G1 to the zero inputs in parallel. This clears the output register for the purpose of receiving new computer data. At the same time, the "read out" flip-flop is driven to the opposite state, which applies an enabling signal to the 12 parallel output gates. The data bits in the 12 right-most positions of the computer's right Accumulator are then transmitted in parallel to the output converter register, where they are held until the end of the next computation. The analog output voltage is synthesized from the contents of the output register by means of the decoder circuits previously described.

Input conversion is initiated by applying the pulse from G1 to the first monostable multivibrator of the input-converter register, as described in Chapter V. Upon completion of input conversion, an "input conversion complete" pulse appears at the output of the analog-to-digital converter. This pulse is simultaneously applied to the "read out" flip-flop, the "read in" flip-flop, the Storage Insertion Register (SIR) of the computer, and a two microsecond delay circuit. The "read out" flip-flop immediately reverts to its initial state. This results in the removal of the enabling signal to the 12 read-out gates.

The "read in" flip-flop is driven to its opposite state. This applies an enabling signal to the 12 parallel read-in gates. At the same time, the SIR is cleared to the zero state by applying the "input conversion complete" pulse to the proper inputs. After a two microsecond delay to allow the contents of the analog-to-digital converter register to be transferred to the SIR, the "input conversion complete"

pulse is applied to computer amplifier V4905, where it appears as an "initiate write" pulse. This causes the computer to store the contents of the SIR in the memory location specified by the programmer in the execution address of the "76" command.

When the computer has completed storage of the input data, a "has written" pulse appears at the output of computer amplifier V1501. This pulse is simultaneously applied to the "read in" flip-flop and the "computer stop" flip-flop. The "read in" flip-flop is driven back to its initial condition. This removes the enabling signal from the 12 read-in gates. The "computer stop" flip-flop is also driven to its original state and an enabling signal is again applied to the "computer stop" gate, G2. This allows the flow of computational clock pulses to the computer to resume, and the computer proceeds with the program.

Circuit construction.-- Solid-state flip-flops, gates, and delay circuits available at the Rich Electronic Computer Center can be used in the construction of the control circuits shown in the block diagram of Figure 19.

CHAPTER VII

CONCLUSIONS

Converter versatility.-- As improved solid-state devices appear on the market, it should be possible to build analog-to-digital and digital-to-analog converters of the type described in this study with ever-increasing accuracy and conversion speed.

While the converters described were designed for use with a large-scale digital computer, the possibilities for real-time computation utilizing specialized high-speed digital computers should not be overlooked. Because of the high computational accuracy of digital arithmetic units, such units should prove particularly useful when used in conjunction with analog control systems or analog computer simulation problems. Using advanced logic modules, magnetic core memories, and high-speed flip-flops and gates, such specialized computers should be capable of computations at a clock rate in the megacycles per second region. In these instances, renewed emphasis would have to be placed upon speed of operation of the input and output converters. Speeds considerably higher than those obtainable at present would become a necessity.

Digital function generators are particularly adaptable for use with the converters described. Analog computer simulation problems frequently require the use of unusual functions, but accurate, high-speed function generators are not easy to obtain. Recently, much

discussion concerning specialized digital function generation has been forthcoming from simulation conferences (17). Digital function generation should provide the analog simulation engineer a powerful and versatile tool.

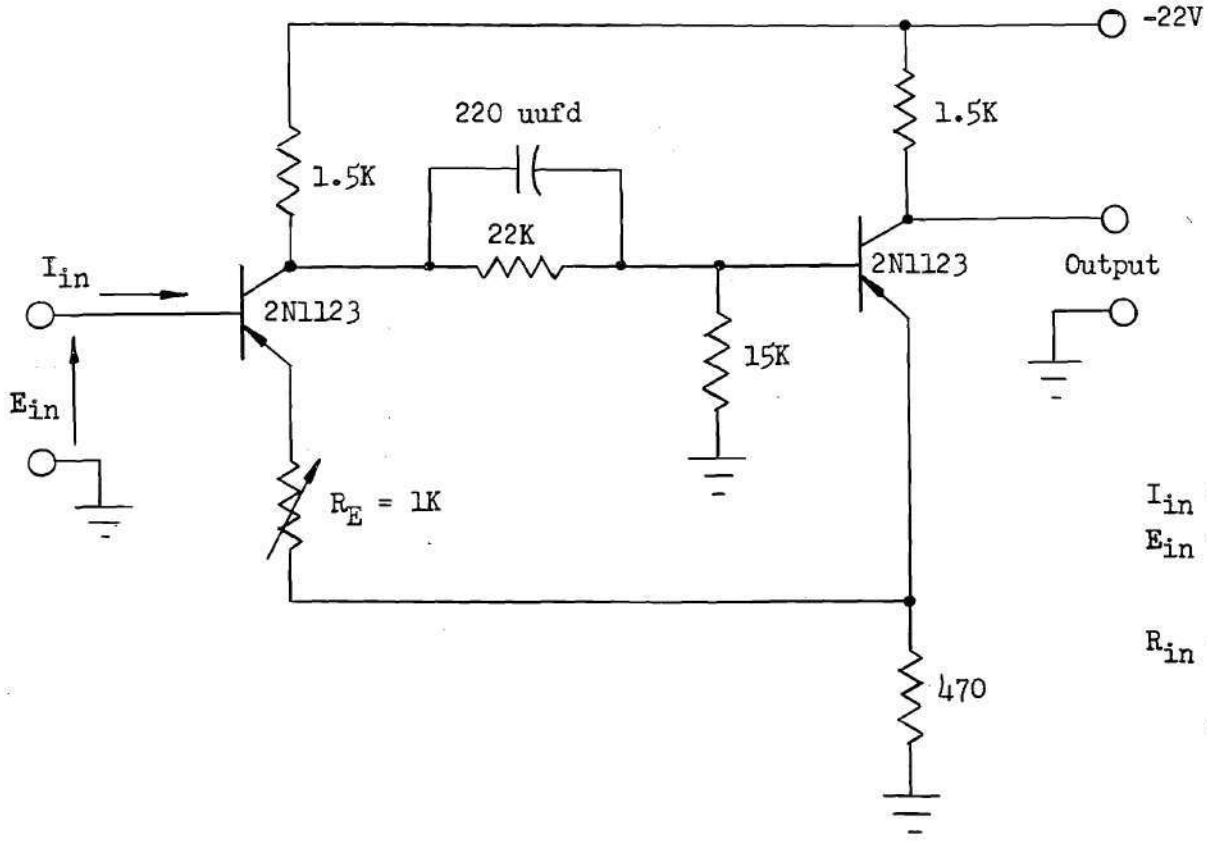
Real-time computation. -- Because of the memory capabilities and command versatility of the ERA 1101 computer, that computer should prove particularly valuable in the study of real-time digital computation in conjunction with continuous systems. There are large areas of interest in the theory of sampled-data systems which remain to be investigated (17). The use of an analog computer in conjunction with a digital system which can be programmed to control the sampling rate would provide the engineer with a versatile laboratory model in such investigations. So-called "adaptive" control systems are of particular interest at the present, and these provide one area of immediate usefulness for such a combination. Thus, it is felt that the addition of the converters and control circuits necessary for such computations would be a valuable addition to the ERA 1101 computer.

APPENDIX A

ZERO-HYSTERESIS SCHMITT TRIGGER CIRCUIT

A transistorized version of a zero-hysteresis Schmitt trigger circuit as shown in Figure 20 was designed and tested in the laboratory (18). Design procedure basically followed that described in the literature, with the exception of the addition of R_E (19). Consider E+ to be the voltage which drives Q1 to the "on" state and E- to be the voltage which drives Q1 from the "on" state back to the "off" state. If $R_E = 0$ and an input is applied which is slightly greater than E+, Q1 will be driven to the "on" condition. If the applied voltage is reduced such that it is somewhat lower than E+, Q1 remains "on". It is necessary to reduce the input to E- to cut off Q1. This is because the base to emitter voltage of Q2 when Q1 is "on" is lower than when Q1 is "off", while the emitter voltage has changed little. Thus, Q2 remains cut off when the input is reduced slightly below E+. In order to bring Q2 into conduction, the input must be reduced to E-. The addition of R_E has no effect on E+ so far as Q1 is concerned, since Q1 is cut off and there is no voltage drop across R_E. For zero hysteresis, E+ must equal E-, and R_E is determined assuming an input of E+ volts for Q1 at cutoff.

R_E = 600 ohms was found to produce zero hysteresis in the laboratory circuit. The circuit is somewhat dependent upon individual transistor characteristics; hence, R_E should be chosen for each circuit constructed. Cut-on and cut-off voltage was 8.0 volts and the input impedance at the transistion point was found to be 285,000 ohms.



I_{in} = 30 microamps

E_{in} = 8 volts

$$R_{in} = \frac{8}{30 \times 10^{-6}}$$

= 285K ohms

Figure 20. Zero-hysteresis Schmitt Trigger Circuit

APPENDIX B

COMPARATOR

In order to evaluate resolution obtainable in the comparator of the analog-to-digital converter, the circuit shown in Figure 21 was set up in the laboratory. It was desired to obtain a pulse output whenever the input voltage at "B" exceeded that at "A". The circuit of Figure 22 was utilized to provide inputs at "A" and "B" varying between 5.0 microvolts and 1.000000 volts. It was also possible to vary the difference in voltage between "A" and "B" over the same range.

With R_E removed and the emitters of Q1 and Q2 connected directly to the collector of Q3, the poorest resolution obtained with eight different combinations of three different transistors was found to be 325 microvolts. With R_E inserted and properly adjusted, the poorest resolution obtainable with the same transistors was 50 microvolts, and the best resolution obtainable from one of the other combinations was 25 microvolts. All measurements were made with a Millivac DC vacuum tube voltmeter.

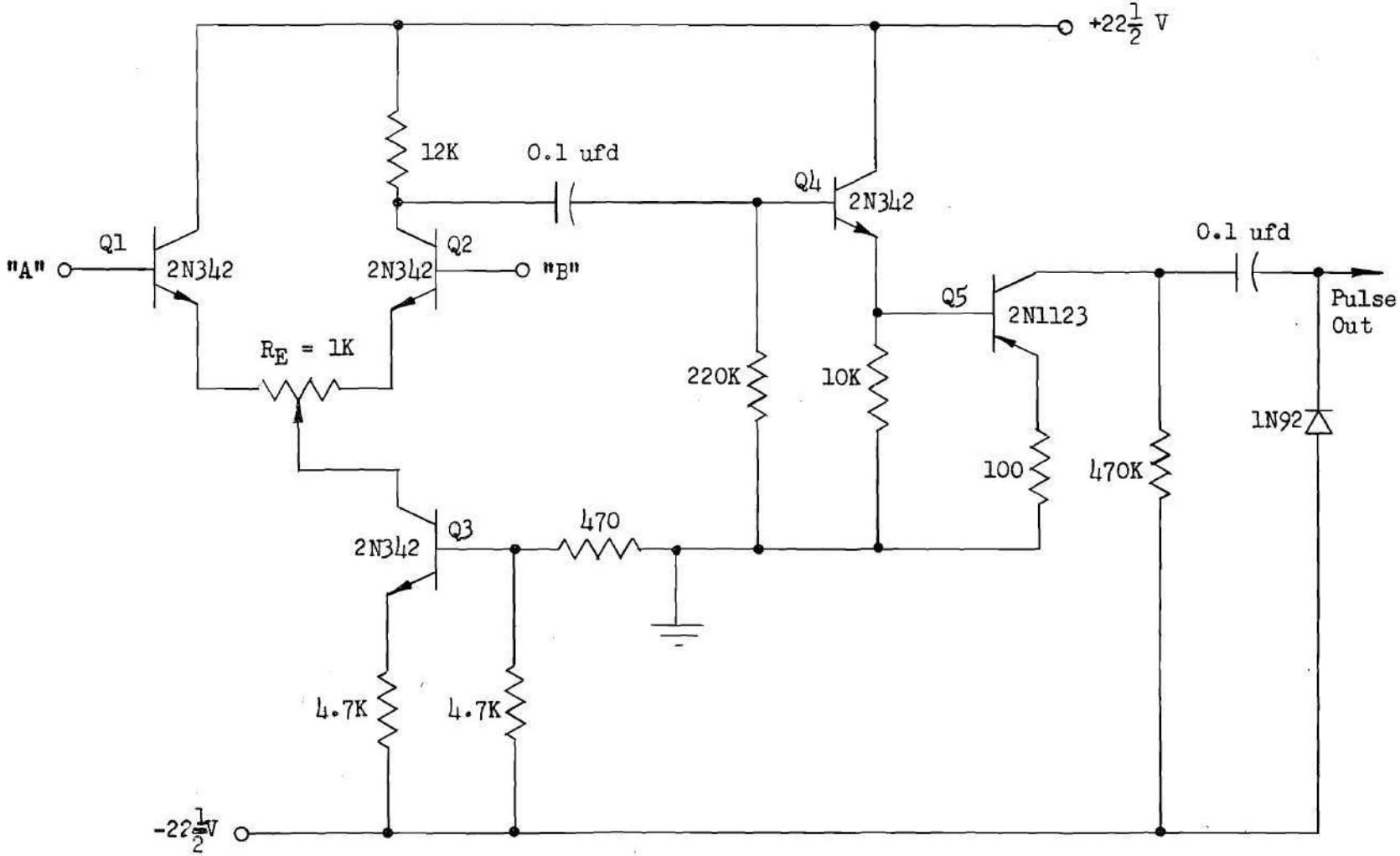


Figure 21. Laboratory Comparator Circuit

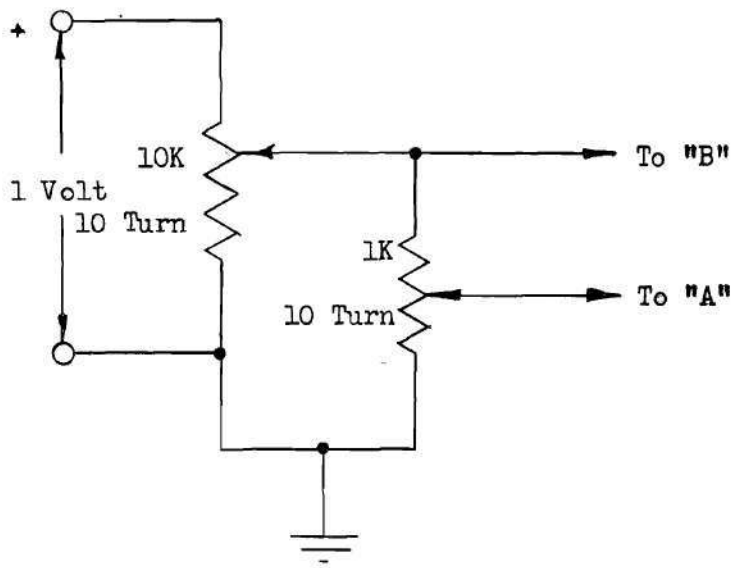


Figure 22. Input Difference Signal

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